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Speed Control of Two-phase A.C. Induction Motors

K. H. WILLIAMSON
Mullard Central Application Laboratory

Theoretical and practical aspects of induction motors are briefly examined, and two methods of speed control are compared. For most applications a speed range of 20 : 1 is adequate, but 50 : 1 can be achieved.

A complete a.c. motor control system, incorporating thyristors and other semiconductor devices, is described in detail, including frequency-to-voltage conversion, and auxiliary features such as acceleration control, current limit and overload protection circuits.

Thyristors used economically with a.c. motors of powers from 1hp to 5hp on two-phase supplies are recommended where low cost is a governing factor. For higher powers three-phase inversion methods will have wider applications.

Estimated costs and relative requirements, such as low costs against higher efficiences with wider speed ranges, of two-phase and three-phase a.c. motor control systems, are compared with equivalent d.c. motor control systems.

INTRODUCTION

The simple robust construction and low maintenance requirements of the squirrel cage induction motor have made it the most widely used electric motor. It has applications ranging from domestic appliances to large industrial drives.

As the induction motor is a fixed speed machine when used on a normal a.c. supply, it has until recently had limited use in applications requiring variable speed. Special applications where it is necessary to use a motor without brushgear, for example in explosive atmospheres, have in the past been satisfied by a variable frequency system using rotating machinery, which is both expensive and cumbersome.

For many years it has been possible to build variable frequency inverters using thyratrons. However, such systems were not practical owing to the high capital and replacement costs; for example, a 12A thyratron costs about £50, and eleven of these in a variable frequency drive would cost £550 for power devices alone which have to be replaced every one to two years. Thyristors cost about one-tenth of these figures and, when used within their ratings, should have an indefinite life. The thyristor variable frequency drive is therefore an economical proposition.

Electronic control in the industrial power field is being introduced at a rapidly increasing rate. This is almost entirely due to semiconductor power devices being more versatile and economical than other means of power control.

TWO-PHASE SYSTEMS

This article is the first of a series on a.c. motor control and it includes a section on the induction motor theory applicable to speed control. A practical 1 hp two-phase variable frequency drive is described in detail. A two-phase system was chosen for the initial study because fewer thyristors are used than in a three-phase system. The two-phase motor is a standard motor except for centre-tapped windings. The control circuits are suitable for three-phase systems with slight modifications, and may be used for motor drives of higher horsepowers. The relative merits of the two- and three-phase methods are discussed and a possible approach for the development of a three-phase system is given.

Two methods of induction motor speed control are compared, variable voltage and variable frequency, the choice of system being dependent upon the application. The variable voltage method is ideally suited to loads such as fan control, where the torque requirement is low for low speeds, but is very inefficient for loads requiring high torques over the whole speed range. The variable frequency system is suitable for all loads but is not as simple as the variable voltage system and is, therefore, more expensive. If the variable frequency drive is compared in cost with the d.c. motor drive then for the same horsepower the a.c. system would cost approximately $1\frac{1}{2}$ times the price of the d.c. system including the price of the motors at the present time.

PRINCIPLES OF INDUCTION MOTOR SPEED CONTROL

Before plunging into the depths of a.c. induction motor speed control it is worth spending a little time going over

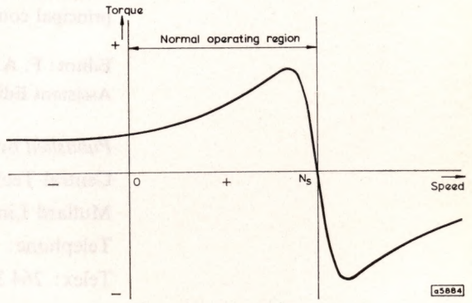


Fig. 1—Torque-speed relationship of an induction motor

the well-known but often forgotten characteristics of induction motors working on sinusoidal supplies.

The full torque-speed relationship of an induction motor is shown in Fig. 1.

The normal operating region for induction motors on fixed frequency supplies is between zero speed and synchronous speed (N_S). However, it is possible to obtain the complete characteristic by driving the motor with external mechanical means both beyond synchronous speed and in the reverse direction. It is important that this characteristic be fully understood and therefore the torque-speed relationship will be considered in greater detail with the aid of the induction motor equivalent circuit of Fig. 2b.

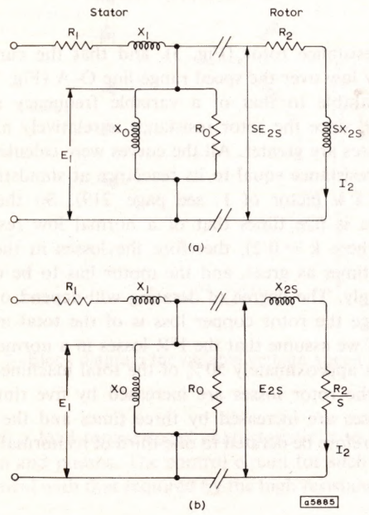


Fig. 2—Induction motor equivalent circuits

The true equivalent circuit is that of Fig. 2a, where the rotor reactance and voltage are the variables, and the equation for rotor current is:

$$I = \frac{SE_{2S}}{\sqrt{(S^2X_{2S}{}^2+R_2{}^2)}} \qquad \ldots(1)$$

where

S = the slip factor = N_2/N_1
E_{2S} = rotor voltage at standstill
X_{2S} = rotor reactance at standstill
R_2 = rotor resistance.

This can be rearranged to:

$$I = \frac{E_{2S}}{\sqrt{(X_{2S}{}^2+[R_2{}^2/S^2])}}. \qquad \ldots(2)$$

Whereas in Eq.1 the variables were E_{2S} and X_{2S}, in Eq.2 the variable is R_2. Although it is not easy to visualise the electrical action of the motor with the current equation in this form it simplifies the equivalent circuit and is generally accepted. The modified equivalent circuit therefore becomes that shown in Fig. 2b.

Let a start be made somewhere in the negative speed region where the rotor is being driven by say another motor in the opposite direction to that of the stator field. The components R_1 and X_1 (Fig. 2b) are almost unaffected by this mode of operation, because the currents through them are still at the supply frequency.

The currents through X_2 and R_2 are greatly affected because both X_2 and E_2 are functions of the slip frequency. The slip frequency in this instance has a value equal to the synchronous frequency plus the equivalent frequency at the negative speed chosen, therefore the slip frequency is high. Consequently, the value of X_2 is high, and because R_2 is initially low and therefore has little effect on the motor currents at relatively high slip frequencies, the rotor current I_2 is limited by X_2 and so the values of torque available under these conditions are very low.

Now consider that the negative speed driving force is adjusted, such that the motor whose characteristic is being investigated is forced to come to rest. The slip frequency has now been decreased to a value equal to the synchronous frequency; that is, a slip factor of 1 has been achieved. As the slip frequency has been decreased, X_2 is also lower and so the available torque is correspondingly higher. This relationship of increasing available torque with decreased slip frequency continues until the motor frequency falls to such a value that the voltage induced in the windings is below that which will increase the current as the value of X_2 decreases.

If the speed is increased beyond N_S (synchronous speed) by again driving by external means, the slip is now negative; and because the slip frequency largely determines the torque-speed relationship, the shape of the characteristic above N_S is almost identical to that between zero speed and N_S, but it is negative and reversed, as was seen in Fig. 1. This means that the motor when driven above synchronous speed reverses its normal function as energy converter from electrical to mechanical energies and becomes an asynchronous generator, and if connected to a normal sinusoidal supply the energy from the external driving machine is fed back as electrical energy into the supply. This condition is important when the braking action of the motor under variable frequency conditions is considered in *Braking* (page 219).

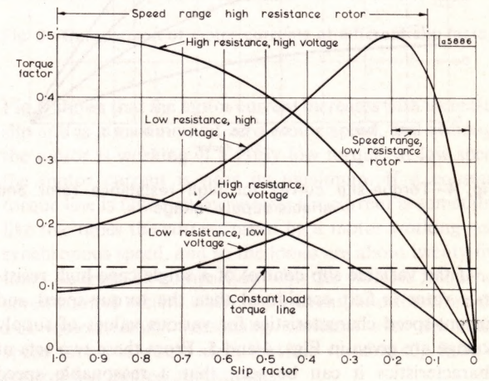


Fig. 3—Relative speed control ranges for variable slip system for high and low values of R_2 open loop

Methods of Speed Control

The speed of an induction motor may be varied in two ways, by varying either the supply voltage or the supply frequency.

First consider varying the supply voltage. Fig. 3 shows the torque-slip relationship for an induction motor for two values of supply voltage and motor resistance. With this method of control using a high resistance ($R_2 = X_2$) motor it is possible to obtain a very wide range of speed, but because of the high resistance of the motor, the efficiency is poor. This method of control is normally limited to motors of less than $\frac{1}{2}$hp, and is frequently used for fan control. More information about this method of control is given in *Speed Control by Variable Voltage*.

The second method, by variable frequency, is a much better way of controlling the speed of induction motors, but until recent years the production of a variable frequency supply required either rotating machinery or rather bulky and expensive thyratron circuits. Consequently, except for special applications, it is only since the advent of the thyristor used in conjunction with the transistor that the variable frequency supply has become a practical proposition. This method of speed control is dealt with in greater detail in *Variable Voltage, Variable Frequency* (page 218).

Speed Control by Variable Voltage

Speed control by variable voltage is normally achieved by varying the supply voltage to the motor, which is usually fitted with a high resistance rotor but under certain conditions may have a standard low resistance rotor.

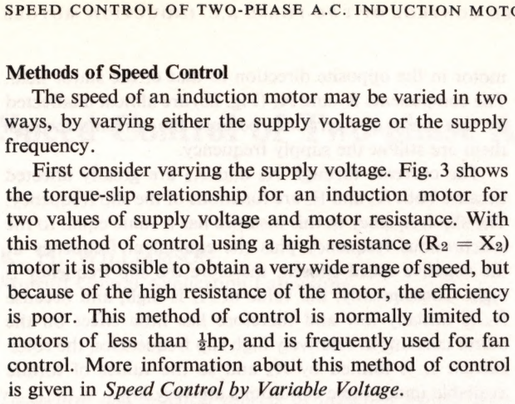


Fig. 4—Torque-slip curves for high resistance rotor and variable supply voltage

If the variable slip control of a single cage high resistance rotor is first considered then the torque-speed and current-speed characteristics for various values of supply voltage are given in Figs. 4 and 5. From these two sets of characteristics it can be seen that a reasonable speed range is obtainable although the maximum speed value for a high resistance rotor is somewhat lower than that for

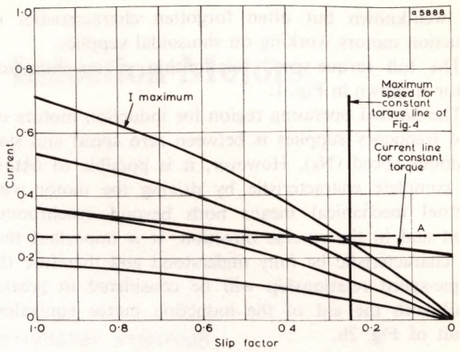


Fig. 5—Current-slip curves for high resistance rotor and variable supply voltage

a low resistance rotor (Fig. 3), and that the current is relatively low over the speed range line O–A (Fig. 5), and is comparable to that of a variable frequency system. However, since the rotor resistance is relatively high the rotor losses are greater. All the curves were calculated for a rotor resistance equal to its reactance at standstill (that is, with a k factor of 1: see page 219). So the rotor resistance is five times that of a normal low resistance rotor (where $k = 0{\cdot}2$), therefore the losses in the rotor are five times as great, and the motor has to be derated accordingly. The degree of derating will depend on what percentage the rotor copper loss is of the total machine losses. If we assume that the I^2R losses in a normal rotor represent approximately 50% of the total machine losses, then if the rotor losses are increased by five times, the total losses are increased by three times and the motor must therefore be derated to one-third of its normal rating.

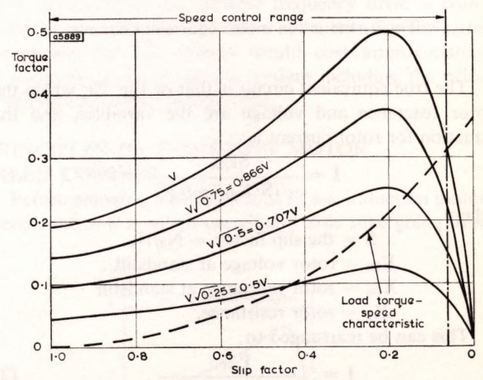


Fig. 6—Torque-slip curves for variable voltage open loop, fan type load

It is possible to use normal low resistance rotor machines on variable slip speed control, either under closed loop conditions or on open loop, with particular load torque-speed characteristics. Fig. 6 shows a suitable torque-speed characteristic of the load with respect to

that of the motor. By varying the supply voltage to the motor it is possible to vary the motor speed over the range shown. Each speed setting is a stable condition because a change in the load torque is always countered by an opposing motor torque. For a given supply voltage a tendency for the motor speed to rise is halted because the load torque requirement for an increase in speed is greater than the motor can supply. Also a drop in speed causes the load torque requirement to fall below the output torque of the motor and so the set speed is maintained.

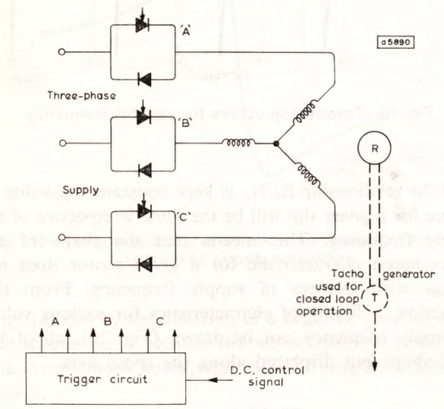


Fig. 7—Block diagram for variable voltage speed control

Such a load torque-speed characteristic is to be found on fans and pumps. The control circuit for such a system is identical with that required by the high resistance motor, Fig. 7.

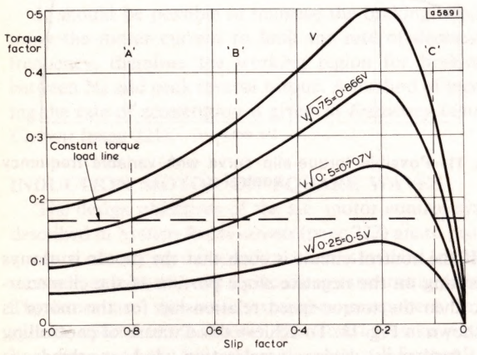


Fig. 8—Torque-slip curves for variable voltage control, low resistance rotor on closed loop

To control a constant torque load by variable slip, closed loop operation is necessary. In Fig. 8, three speed settings are shown. If setting 'B' is taken, then to maintain this speed the supply voltage must be 0·707 times the value of supply volts for maximum speed. If the motor speed is sensed by some means, for example a tachometer on the motor shaft, and the output voltage of this tachometer is compared with a reference voltage, any error signal used in the right sense to control the supply voltage would cause a change in the supply voltage to oppose a change in motor speed. This is normal closed loop practice as used on most control systems.

If with setting 'B' the motor speed tends to rise, the supply voltage is made to fall until the speed has returned to the set value. If the speed drops, the supply voltage is automatically increased to compensate. Therefore, although the motor speed is within what is normally considered the unstable region of its torque-speed characteristic, the closed loop system modifies the motor characteristic to match that of the load.

The system will have to be carefully designed to overcome instability owing to the changes in loop gain over different sections of the torque-speed characteristic.

Variable voltage would at first sight seem to be the complete answer to a.c. induction motor speed control since it is much simpler than variable frequency control and is in some respects simpler and cheaper than d.c. motor control, especially if the cost of the motor is taken into consideration. However, there is one serious drawback, and that is increased motor losses at low speeds.

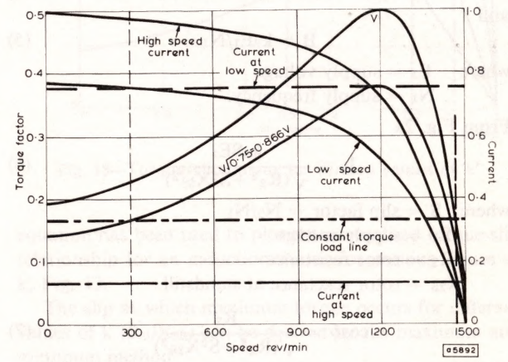


Fig. 9—Comparison of motor currents at different slip factors

Fig. 9 shows that the motor current increases with increased slip and is a maximum at zero motor speed, and although the motor is working at a fairly low torque, at low speed the motor current is near its maximum. If a constant torque line is taken at low speeds, the current is something like five times the current taken by a motor working near synchronous speed, and so the losses are about twenty-five times as great. In comparison with the variable frequency speed control system where the current, and therefore the I^2R losses, remain reasonably constant over the entire speed range, it would seem that the variable slip form of control has limited applications.

It should be noted that the effect of harmonics on the supply waveform has been ignored.

Variable Voltage, Variable Frequency

The electrical characteristics of the a.c. induction motor can be likened to those of the transformer, and in both cases when the frequency is changed the voltage must also be changed for optimum performance. If the frequency is varied and the voltage kept constant, then below the design frequency, the motor or transformer magnetic circuit will saturate, and above the design frequency, the device is not being used to its fullest capabilities.

For optimum use of the motor, the volt-second product of the supply should be kept constant. In other words, the product of the mean voltage of the supply and the periodic time of the supply frequency should remain constant over the working range of frequencies.

The torque equation developed here is considered further for the purpose of including the supply frequency as a variable and not lumped in with a constant as it generally is.

Consider a conductor of length ℓ, through which a current I is flowing, surrounded by a magnetic field of strength B, then the force on the conductor is $B\ell I$.

The torque on the motor for x conductors is

$$xRB\ell I\cos\phi \qquad \ldots(3)$$

where R = distance of conductor from motor axis
x = number of conductors
$\cos\phi$ = phase angle between B and I
(for further details see Appendix 1).

$$\text{Torque} = k_1 BI\cos\phi \quad \text{where } k_1 = xR\ell \qquad \ldots(4)$$

and

$$B = k_2 E_1/N_1 \qquad \ldots(5)$$

where E_1 = supply voltage
N_1 = supply frequency.

From Fig. 2a

$$I_2 = \frac{k_3 SE_1}{\sqrt{(R_2^2+S^2X_{2S}^2)}} \qquad \ldots(6)$$

where S = slip factor = N_2/N_1
E_1 = supply voltage
R_2 = rotor resistance
X_{2S} = rotor reactance at standstill

$$\cos\phi = \frac{R_2}{\sqrt{(R_2^2+S^2X_{2S}^2)}}. \qquad \ldots(7)$$

Therefore

$$\text{Torque} = k_4\frac{E_1}{N_1}\cdot\frac{SE_1}{\sqrt{(R_2^2+S^2X_{2S}^2)}}\cdot\frac{R_2}{\sqrt{(R_2^2+S^2X_{2S}^2)}} \qquad \ldots(8)$$

$$= k_4\frac{SE_1^2R_2}{N_1(R_2^2+S^2X_{2S}^2)} \qquad \ldots(9)$$

$$= k_4\frac{N_2}{N_1^2}\cdot\frac{E_1^2R_2}{(R_2^2+S^2X_{2S}^2)} \qquad \ldots(10)$$

where k_4 and $\frac{N_2R_2}{(R_2^2+S^2X_{2S}^2)}$

are constants for a given value of slip.

Therefore

$$\text{Torque} \propto E_1^2/N_1^2. \qquad \ldots(11)$$

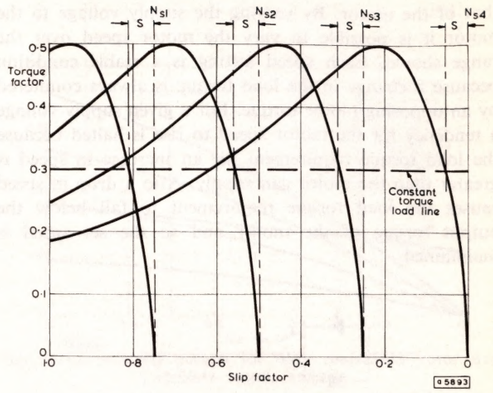


Fig. 10—Torque-slip curves for variable frequency

If the relationship E_1/N_1 is kept constant the value of torque for a given slip will be the same irrespective of the supply frequency. This means that the shape of the torque-speed characteristic for a given motor does not change with changes of supply frequency. From this deduction, a family of characteristics for various values of supply frequency can be drawn (Fig. 10), all of the same shape but displaced along the speed axis.

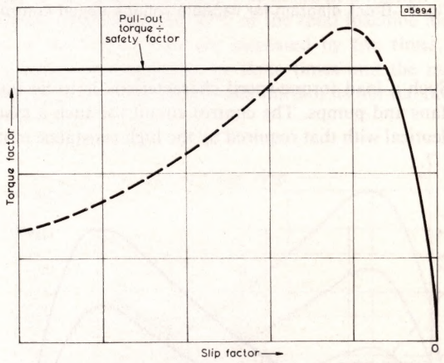


Fig. 11—Possible torque-slip curve with variable frequency control

If the control circuit is such that the motor is always operating on the negative slope portion of the characteristic then the torque-speed relationship for the motor is as shown in Fig. 11. To achieve this a means of controlling the frequency during acceleration and overloads is essential. Details of a system using the motor current as the means for controlling the frequency are given in *Frequency Limit by Current* (page 221).

A motor with such a control system will have approximately twice the acceleration rate and, if the motor does not overheat, overloads up to the pull-out torque are possible at all frequencies.

Braking

The torque-speed relationship (Fig. 1) shows that with the motor speed equivalent to a synchronous speed N_1 less slip, but with the frequency of the motor supply at a lower equivalent synchronous speed of N_2, the torque-speed characteristic of the motor, because of the frequency change, has been shifted down the speed axis by N_1-N_2. By inspection of the characteristics shown in

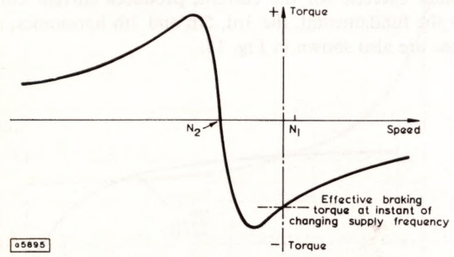


Fig. 12—Torque-speed curve showing braking torque for decreased supply frequency

Fig. 12, and by the insertion of a negative value of slip in the torque Eq.9, because the motor speed is now above the synchronous speed, the value of torque is negative; that is,

$$T = -\frac{k_4SE_1^2R_2}{N_1(R_2^2+S^2X_{2S}^2)}. \qquad \ldots(12)$$

As stated earlier, if the motor were connected directly to a.c. mains, energy under negative torque conditions would be flowing back into the supply and as much negative torque would be available for braking as there was positive torque for acceleration. However, because various power control circuits are between the motor and the supply, the actual braking conditions are more complex.

It should be possible to increase the braking effect by using the motor current to limit the rate of decrease of frequency, therefore the working region for braking is between N_S and peak reverse torque. A method of increasing the rate of acceleration is given in *Frequency Limit by Current* (page 221).

INDUCTION MOTOR ON SQUARE WAVES

The design objectives of the a.c. motor control system described in *System Requirements* (page 222) are to provide a means of varying the speed of a near-standard induction motor in as sophisticated and as cheap a manner as possible. Thyristors are the most expensive component in the system, apart from the motor, therefore as few as possible have been used. To keep down the costs still further it was decided to dispense with quasi square waveforms in the inverters and simply to feed the motor with square waves.

Brook Motors Ltd. have made some measurements of the effect of square waves on an a.c. induction motor. Two complete tests were made on a motor on near-square wave and sinusoidal supplies. Test results for both are reproduced in Tables 1 and 2 at the end of this article. More information is given of the effect of square waves on the torque and current of an a.c. induction motor under the next heading.

Torque and Current

If the torque equation for an a.c. induction motor derived earlier is considered, that is,

$$T = \frac{k_4SE_1^2R_2}{N_1(R_2^2+S^2X_{2S}^2)}, \qquad \ldots(9)$$

and generalising, let $k_4/N_1 = 1$; $X_{2S} = 1$; $R_2 = kX_{2S}$ and $E_1 = 1$,
then

$$T = \frac{Sk}{k^2+S^2} \qquad \ldots(13)$$

In a normal low resistance rotor, the value of k is in the region of 0·1 to 0·2, and in a high resistance rotor k may be as high as 1. The above generalised torque

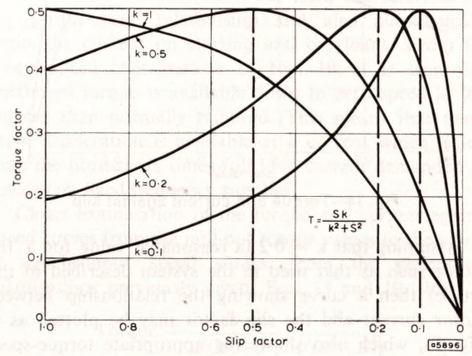


Fig. 13—Torque-slip curves for various values of 'k'

equation has been used to plot the generalised torque-slip relationship for an induction motor for various values of k, Fig. 13.

The slip at which maximum torque occurs for different values of k (R_2/X_{2S}) can be derived by the maximum and minimum method.

$$T = \frac{Sk}{k^2+S^2} \qquad \ldots(13)$$

$$\frac{dT}{dS} = \frac{(k^2+S^2)k-Sk(2S)}{(k^2+S^2)^2} \qquad \ldots(14)$$

at maximum $dT/dS = 0$.

Therefore $$\frac{(k^2+S^2)k-Sk(2S)}{(k^2+S^2)^2} = 0 \qquad \ldots(15)$$

or

$$k^2+S^2 = 2S^2, \quad k^2 = S^2, \quad k = S. \qquad \ldots(16)$$

This means that the maximum torque occurs at a value of slip factor equal to k, the ratio of rotor resistance to reactance. This fact may be observed in Fig. 13.
Substituting k = S in Eq.13 gives:

$$T = \frac{S^2}{2S^2} = 0{\cdot}5. \qquad \ldots(17)$$

This is the value of maximum torque as given in the generalised torque-slip characteristics in Fig. 13.

A similar exercise is possible for the motor current and supply current since there is a direct relationship between the two, therefore $I_2 = k'I_1$.
Since

$$I_2 = \frac{SE_1}{\sqrt{(R_2^2+S^2X_{2S}^2)}}, \qquad \ldots(18)$$

and generalising let $E_1 = 1$; $X_{2S} = 1$ and $R_2 = kX_{2S}$, then

$$I_2 = \frac{S}{\sqrt{(k^2+S^2)}}. \qquad \ldots(19)$$

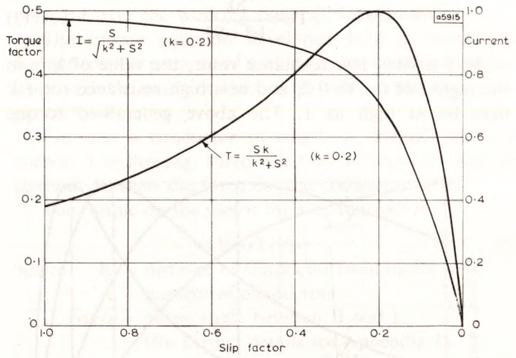


Fig. 14—Torque and current against slip

Assuming that k = 0·2 (a reasonable value for a 1hp motor such as that used in the system described in this article) then a curve showing the relationship between motor current and the slip factor may be plotted as in Fig. 14, which also shows the appropriate torque-speed curve.

Now that the validity of these generalised equations has been established, it is possible to determine the torque available from an induction motor with non-sinusoidal supplies.

The voltage waveform supplied to the motor in the system described is square and the harmonic equation for a square waveform is:

$$v = V_{max}\frac{4}{\pi}\left(\sin\theta + \frac{1}{3}\sin 3\theta + \frac{1}{5}\sin 5\theta + \frac{1}{7}\sin 7\theta + \ldots\right).$$

Separating the harmonics and calculating the torque values for each, produces the curves shown in Fig. 15. A similar exercise for the current, produces current curves for the fundamental, the 3rd, 5th and 7th harmonics, and these are also shown in Fig. 15.

Fig. 15—Torque and current against slip for fundamental and harmonics of a square wave

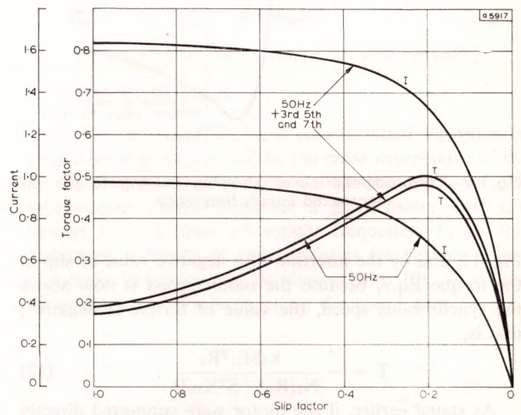


Fig. 16—Fundamental and square wave torque and current against slip

Addition of the harmonic values of current and torque to their respective fundamental values gives the relationship shown in Fig. 16, where the effective torque-speed and current-speed curves for a square wave supply are compared with those of the fundamental alone. Going a stage further, curves were plotted of percentage increases in torque and current, due to the harmonics, on the fundamental values. These curves are given in Fig. 17. For the speed corresponding to 5% slip (normal full load slip value) they show that for a decrease in torque of 8% due to the harmonics there is an increase of 145% in current. So although the harmonics subtract from the output torque of the motor there is a considerable increase in current.

The efficiency of the motor is $\eta = \dfrac{\text{output}}{\text{input}}\,100\%$

where $\text{output} = \dfrac{2\pi TN}{33\,000}\ \text{hp} \qquad \propto TN$

and the $\text{input} = 2\,VI\cos\phi \qquad \propto I\cos\phi$

therefore $\eta \propto \dfrac{TN}{I\cos\phi}\,100\%.$

If it is assumed that for a given speed the power factor $\cos\phi$ is a constant, then the depreciation in efficiency due to the addition of the harmonics can be calculated from

$\Delta\eta = \Delta T/\Delta I$ and when plotted gives the characteristic shown in Fig. 18.

It should be noted that the foregoing calculations are very approximate and only first order effects are taken into account.

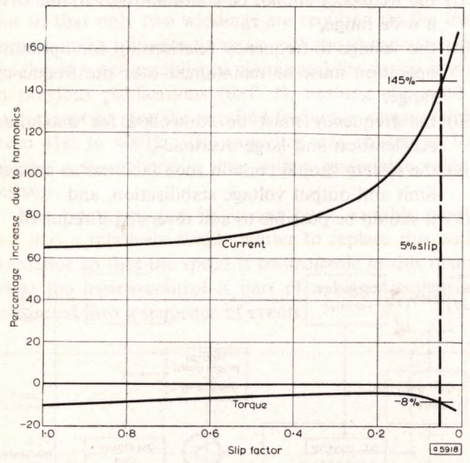


Fig. 17—Percentage increase on torque and current

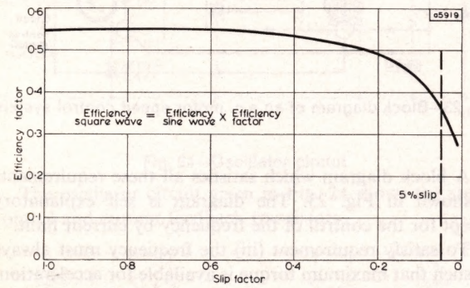


Fig. 18—Efficiency factor against slip factor

Frequency Limit by Current

To use the variable frequency system to the full, it is desirable to ensure that the value of slip never exceeds that at which pull-out torque occurs. In other words, the motor always operates on the negative slope of the characteristic. This can be achieved by measuring the slip frequency and converting it into a d.c. signal which is used to control the frequency. However, it was thought that this is not a particularly easy method in practice, so it was decided to use the motor current as the means of controlling the frequency.

The current-speed and torque-speed characteristics are shown drawn to the same speed scale in Fig. 19. If a current I_1 corresponding to a torque T_1 (just below pull-out torque) is chosen as the limit above which the frequency

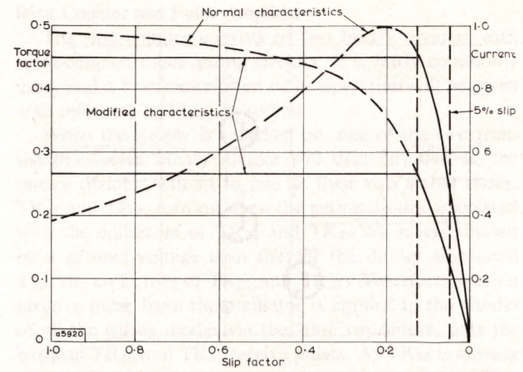


Fig. 19—Torque and current against slip with frequency limit

is reduced, then the two characteristics are modified, as shown in Fig. 19. This offers the ideal characteristic for the torque-speed relationship and also automatically limits the current on starting and overloads. From the torque-speed characteristic of Fig. 19, it is seen that maximum torque is available down to zero speed at less current than normally required. This means that maximum acceleration is available at a current which is less than the normal six times full load current demanded by motors on fixed frequency supplies.

Closer examination of the torque and current against speed curves from the pull-out torque values to the values at synchronous speed shows, from the generalised relationships previously given, Eqs. 13 and 19, that

$$\text{Torque} = \frac{k}{\sqrt{(k^2+S^2)}}\cdot\frac{S}{\sqrt{(k^2+S^2)}} \qquad \ldots(20)$$

$$= \frac{I_2k}{\sqrt{(k^2+S^2)}}$$

$$= \frac{I_2k}{S}.I_2 = \frac{I_2^2k}{S}. \qquad \ldots(21)$$

For small values of slip $I_2 \propto S$, therefore the torque $\propto I_2$. This is verified by plotting I_2 against torque as in Fig. 20.

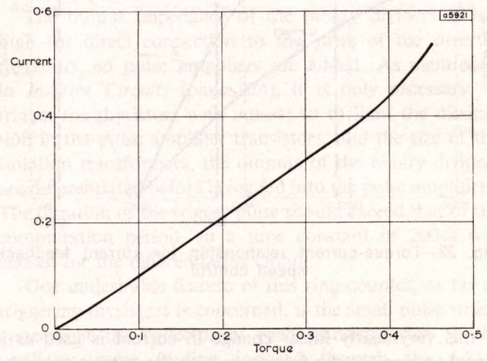


Fig. 20—Relationship between torque and current

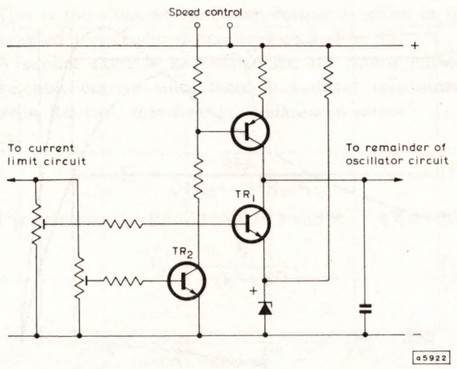


Fig. 21—Frequency limit and compensation circuit

This linear relationship between I_2 and torque is not important for acceleration control, but it is most important if a form of current feedback is used to improve speed regulation.

Frequency Limiting Circuit Techniques

A circuit to perform both the frequency limit by current and the speed regulation improvement functions is shown in Fig. 21. As the motor current rises initially it causes the transistor TR_2 to increase its collector current, thereby increasing the frequency of the oscillator. When the motor current is sufficient to make the input voltage to the circuit large enough to overcome the regulator diode voltage, then transistor TR_1 conducts and decreases the capacitor charging rate, consequently decreasing the oscillator frequency. In other words, as the current increases due to the applied load, the current-speed relationship approximates to a straight line β degrees from a constant speed line through 1500rev/min (Fig. 22).

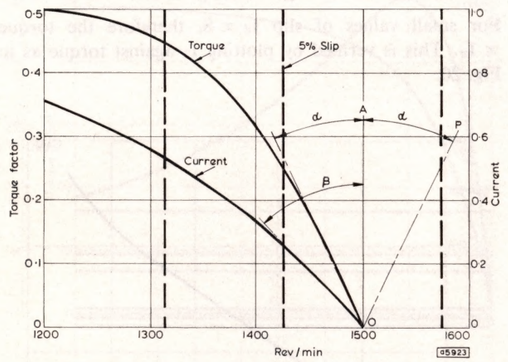


Fig. 22—Torque-current relationship for current feedback speed control

If this very-nearly linear change in current is used as a signal to increase the frequency with the correct gain, the frequency, and hence synchronous speed, will increase with increasing torque along the line O–P, which will cause the torque-speed characteristics to follow the line O–A, indicating a much improved regulation.

SYSTEM REQUIREMENTS

The requirements of a simple but comprehensive a.c. motor control system can be summarised as follows:

(i) the frequency should be continuously variable over a wide range,
(ii) the voltage-to-frequency relationship for optimum operation must be maintained over the frequency range,
(iii) the frequency must be controlled for maximum acceleration and large overloads,
(iv) the system should contain such facilities as current limit and output voltage stabilisation, and
(v) it should be possible to add reversing if required.

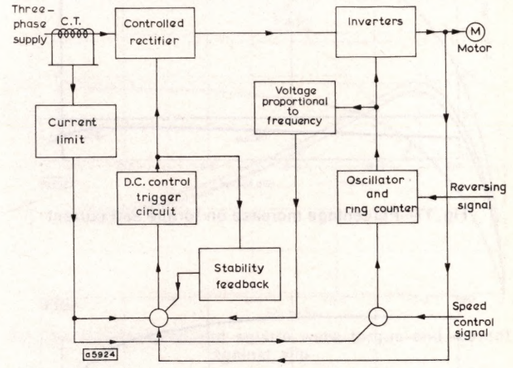


Fig. 23—Block diagram of an a.c. motor speed control system

A block diagram which satisfies all these requirements is shown in Fig. 23. The diagram is self explanatory except for the control of the frequency by current limit.

To satisfy requirement (iii) the frequency must always be such that maximum torque is available for acceleration, and that pull-out torque is never exceeded. The method of frequency control shown in the block diagram uses the motor current to sense the speed of the motor relative to the supply frequency.

The detailed operation of this part of the circuit was given in *Frequency Limit by Current* (page 221).

System Operation

The speed control signal varies the pulse repetition frequency of the master oscillator which determines the operational frequency of the power inverter. The pulses from the oscillator are also fed into the voltage-proportional-to-frequency circuit, the output of which is compared with the inverter output voltage; the error signal goes into the d.c. control circuit to adjust automatically the d.c. voltage into the inverters to satisfy the relationship of voltage-to-frequency.

The current limit signal is fed into the d.c. control circuit to override the voltage control signal in the event of current overload. This signal also controls the oscillator frequency for acceleration and motor overload protection. There is a frequency selective feedback circuit across the d.c. control circuit to prevent instability.

Oscillator

The oscillator (Fig. 24) is the MY5001 blocking oscillator trigger circuit, but with a directly coupled output so that only two windings are required on the transformer, and a transistor in series with the charging resistor. As this is a well-established circuit and the design is given in previous publications (Ref. 1), nothing else need be said except to give the required frequency range which is from 4Hz to 400Hz. The capacitor was chosen as 10μF to give a slow charging time with a reasonable value of resistor.

The frequency can be varied by a variable resistor, but it is a relatively simple matter to replace this with a transistor so that the speed is controllable in this manner when the motor control is part of a bigger system and integrated into a sequence of events.

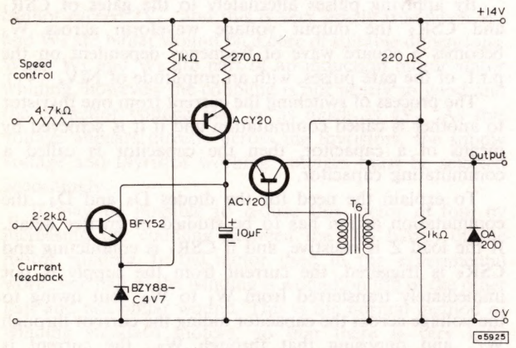


Fig. 24—Oscillator circuit

The oscillator circuit given in Fig. 24 shows the speed control and current feedback transistors.

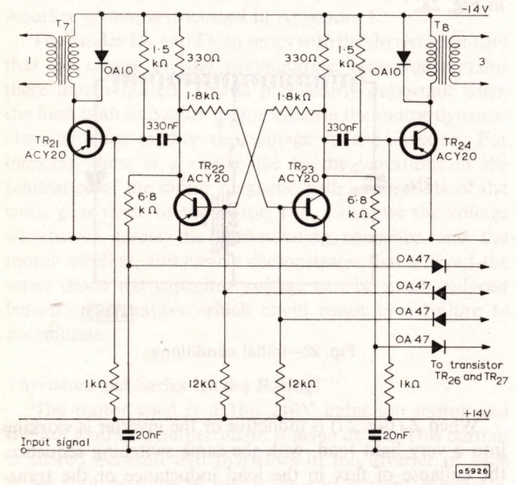


Fig. 25—One half of ring counter plus pulse amplifiers

Ring Counter and Pulse Amplifier

The ring counter consists of two binary dividers with cross-coupled diode-gating circuits. It is fairly commonly used, and a brief description of its operation will be given with reference to Figs. 25 and 50.

When the supply is switched on, one of the two transistors in each binary divider will turn on; that is, the binary dividers will sit in one of their two stable states. TR_{22} and TR_{27} turn on, then the gating diodes associated with the collectors of TR_{23} and TR_{26} are reverse-biased by a greater voltage than that of the diodes associated with the collectors of TR_{22} and TR_{27}. Therefore, when a positive pulse from the oscillator is applied to the anodes of all the gating diodes via the 20nF capacitors, only the bases of TR_{23} and TR_{27} receive pulses. As TR_{23} is already off, the first binary divider remains unchanged; but TR_{27} is conducting when the pulse arrives, and consequently it turns off. TR_{26} is now conducting, so the second binary divider has changed states.

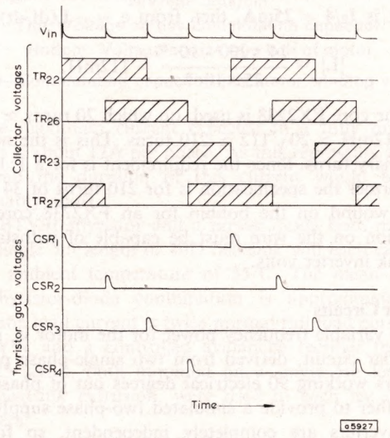


Fig. 26—Ring counter waveforms

The conduction periods of the transistors in the ring counter are given in Fig. 26 in relationship to the oscillator pulses.

The output impedance of the binary dividers is too high for direct connection to the gates of the inverter thyristors, so pulse amplifiers are added. As mentioned in *Inverter Circuits* (page 224), it is only necessary to trigger the thyristors with pulses; so to limit the dissipation in the pulse amplifier transistors, and the size of the isolation transformers, the outputs of the binary dividers are differentiated before being fed into the pulse amplifiers. The duration of the trigger pulse should exceed that of the commutation period, so a time constant of 200μs was chosen for the differentiating circuit.

One undesirable feature of this ring counter, as far as triggering thyristors is concerned, is the small pulse which appears at the collector of each transistor due to the oscillator pulse feeding forward through the 6·8kΩ resistors. This small pulse is sufficiently large to trigger a

sensitive gate thyristor, so it is essential that it is eliminated from the gate signal. The easiest way to remove this unwanted pulse is to put a pedestal voltage on the base of the pulse amplifier transistor, as shown in Fig. 25. The potential divider is calculated to give a reverse base-emitter voltage of about 3V, which is about five times the undesired pulse amplitude.

The value of the coupling capacitor can now be calculated to give a pulse of duration approximately 200μs. If the input impedance of the ACY20 is high compared with the parallel combination of the two potential divider resistors, which is 600Ω, then for a time constant of 200μs

$$C = \frac{200\times10^{-6}}{600} = 330\text{nF}.$$

The pulse transformer has a bifilar winding on a Ferroxcube cup core type FX2238. This is considered to be a good design basis for a pulse transformer because the leakage inductance is very low.

The gate voltage required to trigger a thyristor from the BTY91 series is 10V at 100mA. If the magnetising current is $I_2/4 = 25\text{mA}$, then from $e = -L(dI/dt)$

$$|L| = \frac{14\times200\times10^{-6}}{25\times10^{-3}} = 112\text{mH}.$$

If the core FX2238 is used, on which 20 turns ≃ 1mH, then 112mH ≃ $20\sqrt{112}$ ≃ 210 turns. This is the number of primary turns. Since the requirement is for a 1:1 pulse transformer the specification is for 210 turns of 34 s.w.g. bifilar wound on the bobbin for an FX2238 core. The insulation on the wire must be capable of withstanding the peak inverter volts.

Inverter Circuits

The variable frequency power for the motor is, in this particular circuit, derived from two single-phase parallel inverters working 90 electrical degrees out of phase with each other to provide a simulated two-phase supply. The two inverters are completely independent, so for the purpose of analysis each inverter can be considered separately.

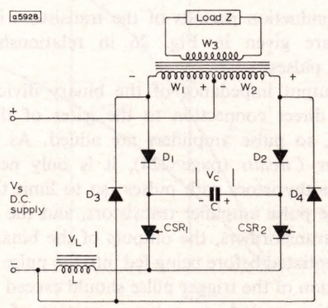


Fig. 27—Basic inverter circuit

In the parallel inverter circuit shown in Fig. 27, the two diodes D_1 and D_2 in series with the thyristors have been added to the conventional circuit for reasons given in the final paragraph of this section.

If thyristor CSR_1 is conducting, then current will flow from the supply through the winding W_1, diode D_1, and back to the supply via choke L. For the purpose of this circuit description, windings W_1 and W_2 will be considered as a centre-tapped primary winding of a transformer the secondary of which is loaded with an impedance Z.

The steady state voltages around the circuit are also given in Fig. 27. The voltage developed across winding W_2 is due to the transformer action between W_1 and W_2. If the voltage dropped across the diodes and thyristors is neglected then the capacitor voltage is $2(V_s-V_L)$ and the load voltage is $N(V_s-V_L)$ where N = turns ratio of the primary and secondary windings = W_3/W_1.

Applying a signal to the gate of CSR_2 causes it to be switched on and the capacitor voltage V_c to appear directly across CSR_1. This action reverse-biases CSR_1 which consequently turns off. Now the current is flowing from the supply through W_2, D_2, CSR_2, and L. The voltages across the windings and the capacitor are equal and opposite to those when CSR_1 was conducting.

By applying pulses alternately to the gates of CSR_1 and CSR_2 the output voltage waveform across W_3 becomes a square wave of frequency dependent on the p.r.f. of the gate pulses, with an amplitude of $N(V_s-V_L)$.

The process of switching the current from one thyristor to another is called commutation and if it is achieved by means of a capacitor, then the capacitor is called a commutating capacitor.

To explain the need for the diodes D_3 and D_4, the commutation action has to be studied in greater detail. If the load Z is resistive, and if CSR_1 is conducting and CSR_2 is triggered, the current from the supply is not immediately transferred from W_1 to W_2, but owing to the voltage across the capacitor aiding the current through W_1, and opposing that through W_2, the current is smoothly transferred at a rate depending on the time it takes for the commutating capacitor C to discharge from $2V_s$ in one direction, and charge to $2V_s$ in the opposite direction. The equivalent circuit for this action is given in Fig. 28.

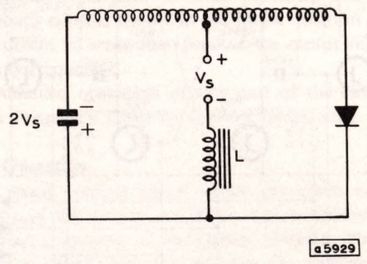


Fig. 28—Initial conditions

When Z (Fig. 27) is inductive or the inverter is working into a very light load, with the same switching sequence, the collapse of flux in the load inductance or the transformer core will try to maintain the current flowing

through W_1. The result of this is that the charge on the commutating capacitor would rise to a value depending on the energy stored in the inductance, and if the current before commutation was high, then V_c is much greater than V_s and may exceed the working voltages of the thyristors.

Diodes D_3 and D_4 clamp the associated halves of the windings to the supply voltages; that is, D_4 ensures that the voltage across W_2 does not exceed V_s, and similarly the voltage across W_1 is clamped to V_s by D_3.

If the inductive coupling between W_1 and W_2 is fairly close, then both D_3 and D_4 effectively clamp both halves of the winding. In other words, if the collapse of flux previously mentioned tries to maintain a current flowing in W_1, but if in order to do so the voltage across W_1 has to rise to overcome the increasing voltage across the commutating capacitor, then the voltage across W_2 also rises. When it reaches the supply voltage, the current is diverted from W_1 to W_2 and flows back into the supply against the supply voltage, and is therefore energy returned.

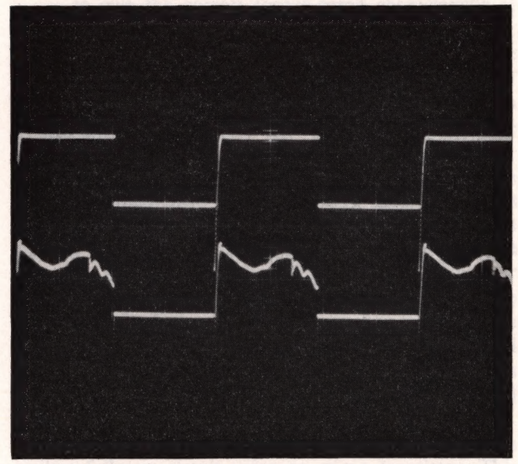
If the coupling between W_1 and W_2 is 100%, then V_c cannot exceed $2V_s$, and this is very nearly true when W_1 and W_2 are bifilar wound on a core of suitable dimensions. When W_1 and W_2 are part of an induction motor stator winding, however, the coupling is not nearly so good and the capacitor voltage may be as much as $4V_s$. As this voltage appears directly across the thyristors, the supply voltage and thyristor working voltages must be selected accordingly.

It may be possible to reduce this factor of four by increasing the coupling between the two halves of the motor winding. In the motor used in the experimental work, one half of the winding is wound on top of the other half and not bifilar wound. This is the normal method of winding standard motors, so that there is very little experience of bifilar winding. But with better insulation and perhaps 'potting' the windings in epoxy resin this problem may be overcome. There is at least one range of motors on the market with 'potted' windings, so bifilar windings would seem to be a practical proposition. Another system is discussed in Appendix 3.

The diodes D_1 and D_2 in series with the thyristors ensure that the charge on the commutating capacitor remains there until required. This is particularly important when the load is an induction motor because the motor dynamic characteristics modify the voltage in the inverter. For instance, there is a ripple due to the variations in the reluctance of the motor magnetic path as the slots of the rotor pass those of the stator. Fig. 29 shows the voltage waveforms across the commutating capacitor and the motor winding, and clearly demonstrates that without the series diode the capacitor voltage can be much reduced before commutation, which could result in a failure to commutate.

Thyristors and Series Diodes Ratings

The motor used is a 1hp 110V induction motor and the full load current per phase is given as 6A. This current is shared between two thyristors in the inverter of each phase, but because of overloads and current transients, 16A BTY91 thyristors were used.



20V/cm: 5ms/cm
Top: Voltage across commutating capacitor
Bottom: Voltage across one half of motor

Fig. 29—Commutating capacitor and motor winding voltages

The maximum current expected in a fully protected system is about 12A per phase. As this represents a 100% overload the duration of this current would be kept reasonably short.

A BTY91 thyristor and a power diode both mounted on a single 5in length of 30D heatsink will each carry 7A at an ambient temperature of 55°C. The mean current per thyristor-diode combination is approximately 6A when the load current is twice normal full load current, so a BTY91 and a controlled avalanche rectifier from the BYX25 series, both mounted on a single 5in length of 30D heatsink extrusion, were used in each leg of both inverters.

The voltage rating of the thyristor should be at least four times the supply voltage plus a safety factor. For a 110V motor, the d.c. supply is about 115V and therefore the voltage across the thyristors is about 460V. In this case at least 700V V_{BO} devices are used. The voltage rating of the series diode must also be of the same order as that of the thyristors, so BYX25–800 rectifiers were used.

The feedback diodes D_3 and D_4 carry surge currents equal in amplitude to that of D_1 and D_2, but the mean level is lower. For the system described, the mean current is a maximum under a light load and never exceeds 5A, so BYX38–900R rectifiers were used.

Commutating Capacitor

The commutating capacitor must hold sufficient charge to maintain the load current without reversing its voltage for a period equal to or greater than the turn-off time of the thyristors.

For a first approximation the load current can be considered to remain constant during the commutation period, so the total charge taken from the capacitor will be Q = It where I is the load current and t is the maximum turn-off time of the thyristors. From the charge equation

$Q = CV_c$, therefore, $C = It/V_c$. If the motor current is a maximum of twice the full load rated current, which in this particular motor is 6A, and the minimum motor voltage is 20V for the lowest speed, then for a maximum turn-off time for the BTY91 thyristors of 50μs, the approximate value of the commutating capacitor is $C = (2\times6\times50\times10^{-6})/(3\times20) = 10\mu F$.

To allow for tolerance on components $2\times8\mu F$ Nitrogol capacitors were used in parallel. The factor 3 in the denominator is the minimum value of voltage magnification due to the lack of close coupling between the two halves of the motor winding, as previously explained. The capacitor used was the Dubilier B215 Nitrogol 600V d.c. working capacitor.

Although it would seem that a.c. working capacitors are necessary, it has been found that d.c. working paper capacitors are quite reliable for most inverter applications. The capacitor charging and discharging currents are quite high but are short in duration. If the terminations within the capacitor are substantial enough to withstand these surges there seems very little need to worry. It is thought that the extended foil type construction is most suitable, giving a sturdy termination and low inductance.

Series Inductance

The purpose of the series inductance L in Fig. 27 is to limit the supply current during commutation. Otherwise the current would rise to relatively high values due to the voltage across the commutating capacitor aiding the supply voltage as shown in Fig. 28. By keeping the current constant, the series inductance aids commutation and enables a smaller capacitor to be used than that which would otherwise be needed.

The inductance must be able to absorb the energy of the capacitor, therefore

$$\tfrac{1}{2}CV_c^2 = \tfrac{1}{2}LI^2$$

or

$$L = CV_c^2/I^2;$$

but

$$C = Q/V = It/V_c,$$

therefore

$$L = V_c t/I.$$

To find the value of inductance, values can be substituted as in the capacitor equation, but this time using the highest supply voltage because this is the worst case:

$$L = \frac{3\times110\times50\times10^{-6}}{12} = 1{\cdot}37\text{mH}.$$

The energy absorbed by the inductor L during commutation is later released as a circulating current round the paths D_3, D_1, CSR_1, and D_4, D_2, CSR_2. Because of this flywheel diode action, the mean level of current in the inductor is greater than that of the supply. This current must be taken into account when designing the inductor. The efficiency of the inverter suffers because of this circulating current, but up to one horsepower it is not considered worthwhile making the circuit more complicated to return this energy to the supply.

When a transformer is used the feedback diodes can be tapped in from each end of the winding. Then the circulating current through each part of the winding produces a voltage across the appropriate half of the winding, and most of the stored energy in the inductor is fed back into the d.c. supply. In the induction motor speed control system the windings are the motor stator windings, so it would be difficult to include tappings.

One advantage of the circulating current passing through the thyristors is that it is only necessary to pulse the gates. The circulating current keeps the thyristors conducting until the load current takes over. This is particularly useful with inductive loads when the current is lagging on the voltage.

Transient Changes in Voltage and Current

The other important ratings of thyristors that have to be considered carefully in switching circuits are the maximum rates of change of voltage and current.

In this particular inverter circuit dV/dt does not present any problems since any supply switching transients are eliminated by the d.c. supply smoothing circuit. The dV/dt generated by the switching action is limited by the charging rate of the commutating capacitor. The maximum dV/dt can be calculated as follows:

$$v = V_{max}\sin\omega t$$
$$dV/dt = -V_{max}\omega\cos\omega t.$$

This is a maximum when t = 0, therefore

$$dV/dt_{max} = -V_{max}\omega = -V_{max}2\pi/T$$

where

$$V_{max} = 4V_s = 440\text{V}$$
$$T = 2\pi\sqrt{LC} = 0{\cdot}93\times10^{-3}\text{ seconds}$$

where

$$L = 1{\cdot}37\text{mH and } C = 16\mu F.$$

Therefore

$$dV/dt_{max} = 440\times2\pi/0{\cdot}93\times10^{-3} = 2{\cdot}97\text{V}/\mu\text{s}.$$

This is the rate of reapplication of voltage after commutation and is well within the maximum permissible value of 20V/μs given in the BTY91 published data. The dV/dt ratings of the thyristors, therefore, present no problems for this particular circuit.

The dI/dt in the circuit is, however, likely to cause trouble unless limited. The dI/dt is greatest round the circuit loop containing the commutating capacitor and the two thyristors. If it is assumed that one thyristor is conducting at the moment when the other is triggered, then the commutating capacitor will start to discharge round the loop through both thyristors, until the thyristor carrying reverse current loses its stored charge and 'blocks'. Until the thyristor that is being turned off actually blocks, the only limit on the rate of rise of current is the loop inductance which is normally quite low.

Measurements have been made of the dI/dt in this loop using a 'non-inductive' resistor made of multi-layers of carbon strips. The results were plotted against supply current (Fig. 30). At maximum anode current the dI/dt value was approaching 100A/μs which is the maximum value given in the published data for the BTY91, therefore it was necessary to add extra inductance in the loop.

To limit the rate of rise of current to 50A/μs, the value for the total loop inductance can be derived in a similar way to that used for the calculation of dV/dt:

$$dI/dt_{max} = -I_{max}2\pi/T.$$

If I_{max} is 100A (which is well within the BTY91

maximum I_{FRM} rating of 140A), then

$$T = 100\times2\pi/50\times10^6$$

and

$$f = 1/12{\cdot}5\times10^{-6} = 80\text{kHz}$$

which is the resonant frequency required of the commutating capacitance and the loop inductance. From $L = 1/\omega^2C$, the total loop inductance to limit dI/dt to 50A/μs is 225nH. As a guide, a 4in length of 20 s.w.g. wire has an inductance of approximately 120nH.

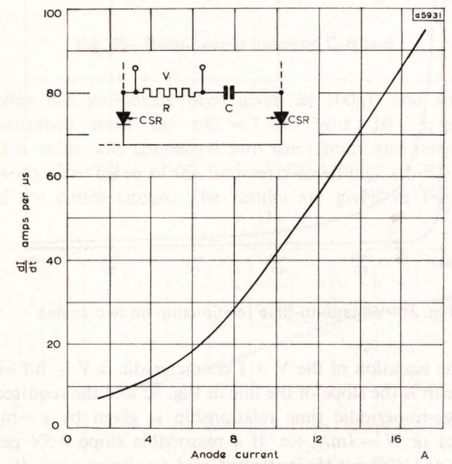


Fig. 30—dI/dt against anode current

Frequency-to-Voltage Converter

The requirements of the frequency-to-voltage converter circuit for a.c. motor control applications are:

(i) it must provide a smooth d.c. voltage output proportional to the frequency of the motor supply; that is, the output frequency of the inverter,

(ii) although the output is very smooth d.c, the response of the system should be very fast,

(iii) it is necessary to boost the voltage at low frequencies for small motors, therefore requirement (i) must be met so that the voltage can be modified to give the correct torque-speed characteristic at low frequencies.

The simplest circuit to satisfy requirement (i) is the well-known diode pump circuit. However, the response of this type of circuit is inherently slow. A digital approach to the problem was considered to be more likely to achieve the above requirements.

The method adopted is that which samples, at a particular instant, the voltage across a capacitor that is discharging at the right V/t relationship. The capacitor is charged to a fixed voltage by the occurrence of an input pulse, and then discharges through a resistor. The capacitor voltage is them sampled and stored until the next pulse arrives, which also recharges the capacitor ready for the next cycle. If the p.r.f. remains constant then the sampled voltage is also constant. When the p.r.f. changes it is immediately detected and the stored voltage is adjusted accordingly.

The stored voltage is connected to the input of an emitter follower circuit using an m-o-s transistor. This circuit, because of its extremely high input impedance, has negligible effect on the stored voltage but gives an output voltage nearly equal to the input voltage at a low impedance.

The circuit, Fig. 31, developed for the motor control system described, is required to work over a range of, say, 1Hz to 100Hz with a possibility of going up to 200Hz. This gives a periodic time of 5ms of which the charging time of the sampled capacitor must be a relatively minor portion. Therefore, allowing 0·25ms for this operation (one tenth of the periodic time of 400Hz, oscillator frequency, see page 223), the component values of the monostable circuit are derived as follows:

The minimum value of capacitor into the m-o-s transistor should be about 10nF. If the main charging capacitor is made ten times this value, or 100nF, then to obtain reasonable charge in 0·25ms the collector load of TR_{19} should be 1kΩ. The total collector current for TR_{19} is therefore

$$14/1{\cdot}33\text{k}\Omega \simeq 10\text{mA},$$

therefore,

$$TR_{19}\text{ max base current} = I_c/\alpha' = 10\times10^{-3}/50$$
$$= 200\mu\text{A}.$$

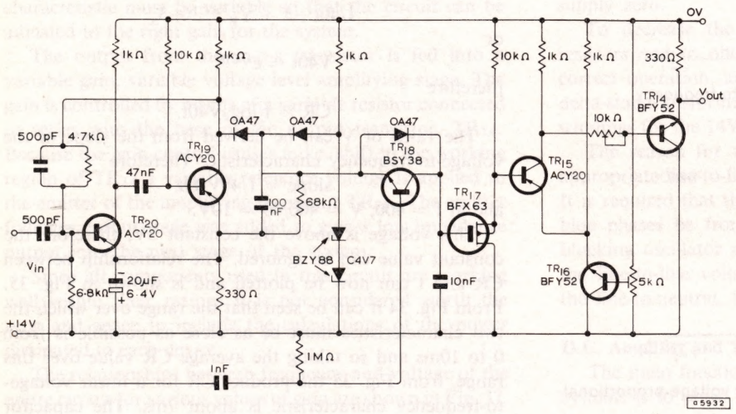


Fig. 31—Frequency-to-voltage converter

This means that a base resistor of 70kΩ or less is required and as the value of this resistor is not critical a value of 10kΩ is used. Therefore to give a pulse of 0·25ms a capacitor of value

$$t/R = 0{\cdot}25\times10^{-3}/10\times10^{3} = 25nF$$

is needed. As this is the minimum value, to allow for capacitor and resistor tolerance a value of 47nF was used, which was found to give over 0·3ms.

The collector load of TR_{20} should be the same as that for TR_{19}. The emitter voltages do not fluctuate when this load is 1kΩ.

The other component values are chosen so that the base of TR_{20} is biased on when TR_{19} is non-conducting.

The sampling transistor BSY38 (TR_{18}) was chosen because of its low leakage characteristics so that the charge on the storage capacitor remains constant between sampling. The on period of TR_{18} is determined by the 1nF capacitor in series with the base, and the forward impedance of the base-emitter circuit. The diode across TR_{18} is to allow the storage capacitor to discharge simultaneously with the 100nF capacitor when the input frequency is decreased.

There is a diode catching circuit to ensure that the 100nF capacitor charges to the same voltage each cycle irrespective of the charge left on it after the previous cycle. This is important, otherwise the linearity of the output is affected.

The p.r.f. range over which this circuit must operate can be derived from the required speed range of the motor. For most applications a 20:1 speed range is adequate. If the motor starts at 1 revolution per second and goes up to 50rev/s (3000rev/min) this speed range of 50:1 is equal to a p.r.f. range of 8 to 400 pulses per second. The pulses are supplied directly from the oscillator which runs at four times the frequency of the inverters as the motor is a 4-pole machine.

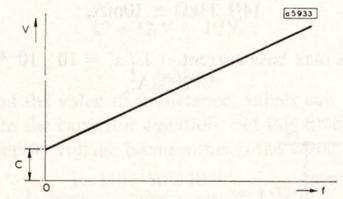


Fig. 32—Voltage proportional to frequency

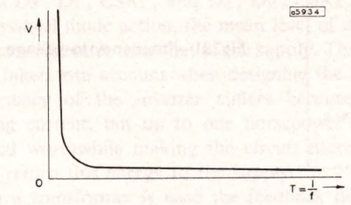


Fig. 33—Voltage-to-time relationship for voltage-proportional-to-frequency

If the required voltage-to-periodic time relationship is studied in greater detail it will be seen that if a voltage proportional to frequency is to be linear (Fig. 32), then the voltage relationship to the periodic time is $V \propto 1/t$ or that of a rectangular hyperbola (Fig. 33).

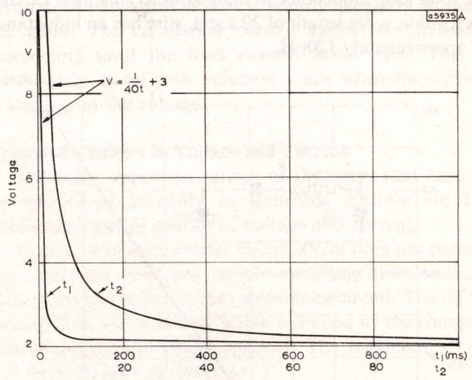


Fig. 34—Voltage-to-time relationship on two scales

The equation of the $V \propto f$ characteristic is $V = mf+c$ where m is the slope of the line in Fig. 32 and the required voltage-to-periodic time relationship is given by $t = m/(V-c)$ or $V = (m/t)+c$. If a reasonable slope 0·5V per 20Hz or 1/40V per Hz is selected, and c as being a standing voltage of 3V, the equation for the relationship of voltage and time becomes $V = (1/40t)+3$. This was plotted and gave the curve shown in Fig. 34. This rectangular hyperbola characteristic is not easy to produce electronically and therefore a substitute had to be found.

As the discharge curve of a charged capacitor, over a limited range, may be approximated to a rectangular hyperbola, then to determine the CR value to produce such a curve the two expressions should be equated as follows.

Rectangular hyperbola $V_c = 1/40t+3$.

Capacitor discharge curve $V_c = V_e^{-t/CR}+c$.

The constant c is 3 for the same limiting conditions of both curves, therefore,

$$1/40t+3 = V_e^{-t/CR}+3,$$

or

$$V40t = e^{t/CR},$$

therefore

$$CR = t/\log_e V40t.$$

The value of V can be derived from the slope of the voltage-to-frequency characteristic. Therefore

$$\text{slope} = 1/40V/Hz$$

and at $f = 400$, $V = 400/40 = 10V$.

This voltage is above the constant 3V, therefore the constant value can be ignored. The relationship between CR and t can now be plotted and is shown in Fig. 35. From Fig. 34 it can be seen that the range over which the two characteristics must be as close as possible is from 0 to 10ms and so taking the average CR value over this range, from Fig. 35 the product CR for a linear voltage-to-frequency characteristic is about 7ms. The capacitor

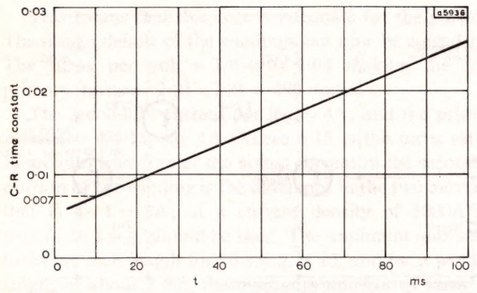


Fig. 35—Relationship between C-R and t

value has previously been given as 100nF and so the resistance must be $t/C = 7\times10^{-3}/0{\cdot}1\times10^{-6} \simeq 68k\Omega$. This value was connected into the circuit and measurements were taken of the frequency-to-voltage relationship of the entire circuit. The results are given in Fig. 36.

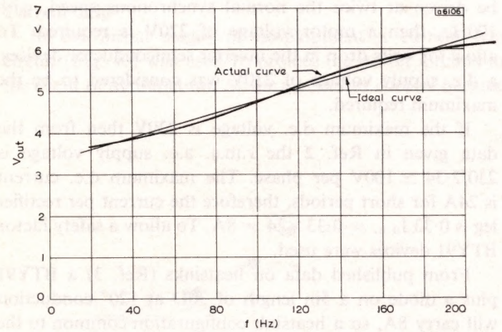


Fig. 36—Frequency-to-voltage characteristic of converter

Although the actual and ideal curves are not quite the same, the differences are small enough to have little effect on the performance of the system.

The Fig. 31 circuit then gives an output voltage proportional to the frequency of the input pulses within reasonable limits. However, before it can be incorporated in the a.c. motor control system the slope of the output characteristic must be variable so that the circuit can be adjusted to the right gain for the system.

The output from the m-o-s transistor is fed into a variable gain, variable voltage level amplifying stage. The gain is controlled by means of a variable resistor connected in series with the base of the output transistor, TR_{14}. Because the gain control causes a d.c. shift in the working region of TR_{14} a variable reference voltage is applied to the emitter of the amplifying transistor TR_{15}. The emitter follower output stage was added to give a low impedance output into the next stage of the system.

Since all components used in this circuit are working well within their ratings it is not considered worth the time and space to include the calculations of the power dissipated in each device.

The relationships between frequency and voltage of the entire circuit for various values of gain are shown in Fig. 37.

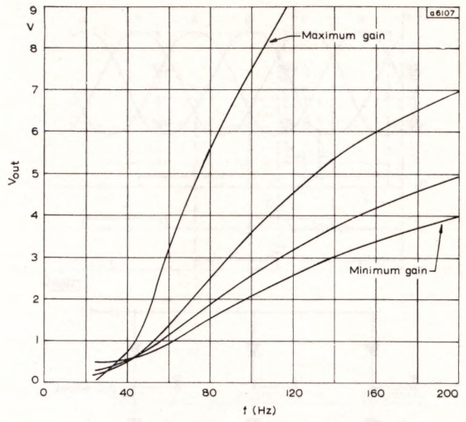


Fig. 37—Frequency-to-voltage characteristics for various values of gain

Three-phase Half-controlled Bridge Trigger Circuits

The requirements for a circuit to trigger the three thyristors in a half-controlled bridge rectifier are, firstly, the trigger pulses for each thyristor must be synchronised to the appropriate phase and, secondly, the trigger angles of all three phases must be controlled from a single d.c. signal such that the differences between the angles of the three phases do not exceed about 20°.

The circuit consists of three blocking oscillators similar to the Mullard standard trigger circuit MY5001 with an ACY20 transistor in each capacitor charging circuit. These three transistors have their bases connected via 10kΩ resistors to a common emitter stage in Fig. 50 so that variations in output voltage of this stage vary the trigger angles of all three blocking oscillators. The blocking oscillators are synchronised to the supply by the usual method of connecting each blocking oscillator across its appropriate phase, and with the aid of a series resistor and a voltage regulator diode using the phase as its supply voltage. Balance between the trigger angles of each phase is achieved by the use of 100kΩ variable resistors between the base of each charging circuit transistor and the supply zero.

To decrease the dissipation in the supply dropper resistors and to obtain the required 30° phase shift for correct operation, as explained in the next paragraph, a delta-star transformer is used. This transformer has extra windings for the 14V–0–14V d.c. supply.

The reason for the 30° phase shift is to obtain the appropriate line-to-line synchronisation as seen in Fig. 38. It is required that the control range for, say, the red and blue phases be from a to b, therefore the appropriate blocking oscillator must be synchronised to this period; the line-to-line voltage must therefore be used and not the line-to-neutral, hence the 30° phase shift.

D.C. Amplifier and Feedback Loops

The main function of a d.c. amplifier in most control systems is to sense the difference between set values and

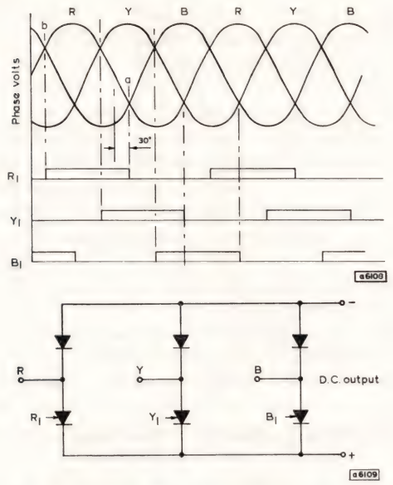


Fig. 38—Trigger periods for thyristors in a half-controlled three-phase bridge circuit

actual values and to amplify the error so that the rest of the system can make the appropriate correction.

The d.c. amplifier of the a.c. motor control system described controls the trigger circuits for the half-controlled bridge that supplies the d.c. to the inverters. The sytem requirements demand that:

(i) the inverter output voltages must vary proportionally to frequency,
(ii) for any particular frequency the inverter output voltage must remain constant independent of load,
(iii) there must be current limit protection.

Consequently there are three control signals and one stabilising signal being fed into the first stage of the amplifier, as shown in Fig. 39.

The output from the frequency-to-voltage converter (TR_{14}, Fig. 31) is fed directly into the emitter of TR_9 as the reference voltage (V_R) and is used for the comparison of the full-wave rectified motor winding voltage.

A voltage proportional to the supply current is fed into the base of the first transistor TR_9 for the purpose of current limit.

Owing to the complexity of the system it was difficult to determine the loop gain required, so the reference voltage proportional to frequency circuit is variable in gain as described in *Frequency-to-Voltage Converter* (page 229).

The feedback circuits are shown in the complete circuit diagram of Fig. 50. The stabilising feedback consists of a common emitter amplifier (TR_{13}, Fig. 50) to amplify and reverse the phase of the feedback signal, and a frequency dependent C–R circuit.

Three-phase Bridge and Supply Transformer

The variable d.c. voltage to the inverters is supplied by a half-controlled bridge connected to a three-phase supply. A fully-controlled bridge would have less ripple, but as this motor control system was to be produced as cheaply

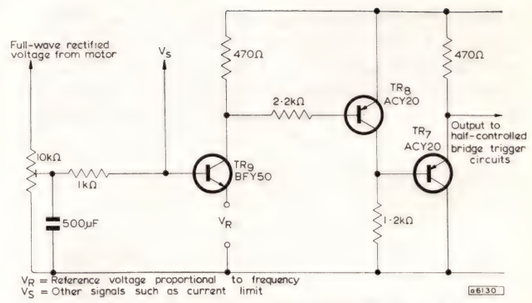


Fig. 39—D.C. amplifier circuit

as possible, six thyristors for d.c. control would have been prohibitive.

The motor supply, for reasons explained in *Inverter Circuits* (page 224), is 110V at 50Hz, so if the motor is to be driven at twice the normal synchronous speed, with 100Hz, then a motor voltage of 220V is required. To allow for volts drop in the inverter semiconductor devices, a d.c. supply voltage of 230V was considered to be the maximum required.

If the maximum d.c. voltage is 230V then from the data given in Ref. 2 the r.m.s. a.c. supply voltage is $230/2{\cdot}34 \simeq 100$V per phase. The maximum d.c. current is 24A for short periods, therefore the current per rectifier leg is $0{\cdot}33\ I_{d.c.} = 0{\cdot}33 \times 24 = 8$A. To allow a safety factor BTY91 devices were used.

From published data on heatsinks (Ref. 3) a BTY91 plus a diode on a 5in length of 30D at 120° conduction will carry 8A, so a heatsink configuration common to the bridge and the inverter can be used.

The voltage rating of the bridge devices need only be 230V plus a safety factor, say 500V.

The supply transformer to drop the voltage from 415V line voltage to 100V can be an auto transformer. Its rating must be about 1kVA for 1hp, but for this particular application it must be capable of supplying 2kVA for short periods. Therefore, if the transformer is designed with the windings rated at 1000A/in² the extra heating at 2kVA will not be excessive.

To determine the size of core needed, the following exercise was gone through for a selection of cores. The flux density for the core material was considered to be a maximum at 16 kilogauss and the cross sectional area of the core finally chosen (Telmag type E E8) was 13·8cm². Therefore the volts per turn for this particular core is $e/n = 4{\cdot}44 \times 16 \times 10^3 \times 13{\cdot}8 \times 50 \times 10^{-8} = 0{\cdot}49$ V/turn.

The window area for this core is $1{\cdot}75 \times 3{\cdot}25 = 5{\cdot}7$in². This space is taken up by two windings, so each winding requires 2·85in². If we assume a copper to insulation and air factor of 0·5 then the total effective window area per winding is $0{\cdot}5 \times 2{\cdot}85$, say 1·42in².

At a current density of 1000A/in², this represents a current of 1420A. Therefore the approximate VA rating of the core is:

$$3 \times 0{\cdot}49 \times 1420 = 2{\cdot}1\text{kVA}.$$

This means that this core is adequate for the purpose. The design details of the windings can now be considered. The turns per volt = $1/0{\cdot}49 = 2{\cdot}04$ making the total primary turns = $2{\cdot}04 \times 240 = 490$ turns.

The secondary current per leg = 4A, and the primary current = $4/4{\cdot}15$, say 1A (where 4·15 is the turns ratio). In an auto transformer the actual current in the secondary portion of the winding is the difference in the two currents, that is $4-1 = 3$A; at a current density of 1000A/in², wire of 16 s.w.g. should be used. The minimum number of turns per inch length for 16 s.w.g. is 15, and for a winding length of about 2·5in, the minimum number of turns per layer = $2{\cdot}5 \times 15 = 37{\cdot}5$. The number of layers = $490/37{\cdot}5 = 13$, and the thickness of winding = $13 \times 0{\cdot}064 = 0{\cdot}835$in.

Summarising, the winding details are: 490 turns of 16 s.w.g. en.cu. wire, tapped at 118 turns for secondary 100V line-to-line. The insulation of the windings of the auto transformer must be suitable for operation on 415V mains.

Current Trip

In the initial stages of development a current trip circuit (Fig. 40) was used to protect the power circuits in the event of malfunction. As the a.c. motor control became

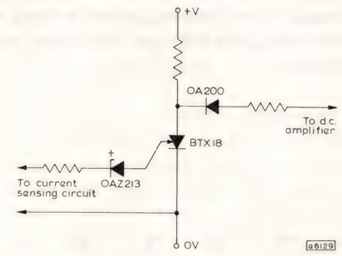


Fig. 40—Current trip circuit used in initial development

more sophisticated there proved to be no further need for the current trip, so it was removed. The current on overload is automatically limited by the acceleration control. The current limit circuit is still included to limit the overload current if the inverters cease to function.

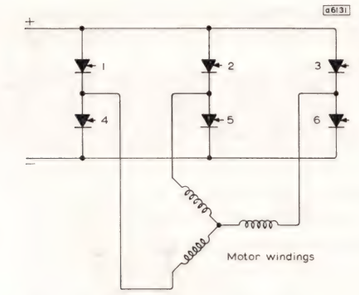
Further developments of a.c. motor control systems may have a current trip circuit instead of a current limit, but this will depend on the application.

OTHER METHODS OF DERIVING VARIABLE FREQUENCY

Four alternative methods of deriving variable frequency will be discussed briefly.

Three-phase Bridge Inverter

The two-phase inverter was adopted for economic reasons and, like most systems produced with cost as an important factor, it has its limitations. The three-phase bridge inverter is better in two important respects; one is that the thyristor voltages never exceed that of the d.c. supply, and the other is the ease with which an output waveform with a lower harmonic content can be produced.



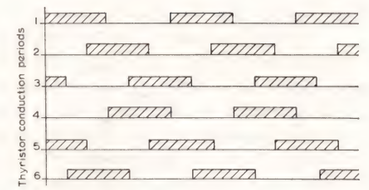


Fig. 41—Thyristor conduction periods for three-phase bridge-connected inverters

A simplified circuit of a three-phase inverter and the conduction periods of the thyristors are shown in Fig. 41. The phase and line voltage resulting from these conduction periods are given in Fig. 42. The line-to-line voltage waveform may be expressed in terms of the fundamental plus harmonics as follows:

$$v = V_{max}\frac{2\sqrt{3}}{\pi}\left(\cos\theta - \frac{1}{5}\cos 5\theta + \frac{1}{7}\cos 7\theta\right)$$

The first predominant harmonic is the fifth. Without the third harmonic, the total harmonic distortion is greatly

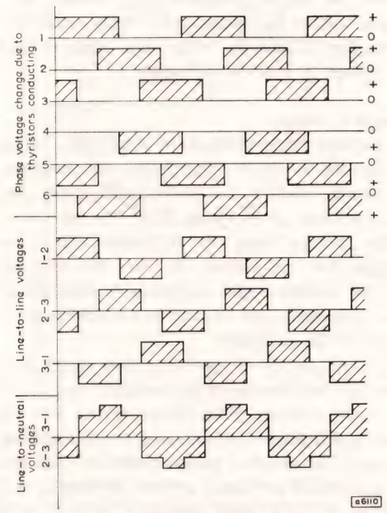


Fig. 42—Phase and line voltages for three-phase bridge-connected inverters

reduced which means that a motor connected to a supply with such a waveform is running under near-sinusoidal conditions.

Only a brief description of the three-phase bridge inverter motor control system is given here to enable a comparison to be made of the two- and three-phase systems.

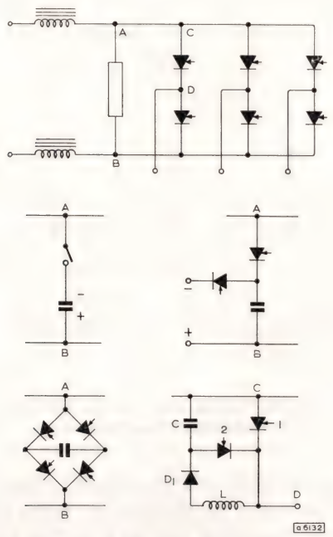


Fig. 43—Commutation methods for three-phase inverters

The thyristors in the bridge circuit of Fig. 41 must be turned off at the end of the required conduction periods, and Fig. 43 shows various methods of reverse-biasing the thyristors either singly or all together. The feedback diodes which are an essential part of the circuit are not shown but they are connected as a three-phase diode bridge such that when the output voltage of the inverter rises above the supply voltage the excess is full-wave rectified and fed back into the d.c. supply, which also tends to clamp the output voltage to that of the supply.

Variable D.C. Supply

Fig. 44 shows three methods of obtaining a variable d.c. supply for the inverters. The first is the half-controlled bridge circuit used in the two-phase system, details of which have been given (page 229). The next is a fully-controlled bridge using six thyristors. There are two advantages that this circuit has over the half-controlled bridge: the output ripple frequency is doubled at lower trigger angles, and it can be used as a synchronous inverter for regeneration purposes.

The third circuit is probably the most interesting because only two thyristors are required and the smoothing is much simpler. This circuit is the d.c. chopper; CSR_1 is turned on and off, causing an interruption of the d.c. supply. The ratio of the on period to that of the off period determines the mean level of the output voltage.

Because this chopping frequency can be made high (1 to 5kHz) the smoothing requirements are much reduced.

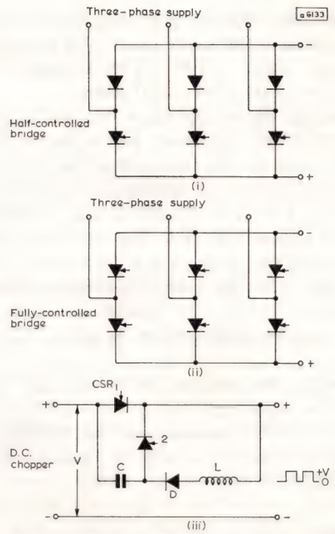


Fig. 44—Three methods of obtaining a variable d.c. voltage

The d.c. input to the chopper can be derived either from a d.c. source such as a battery or by means of diode rectifiers on an a.c. supply. If the response of the control circuits is made fast enough, then the chopper will smooth the input ripple whilst maintaining the mean level of the output d.c. voltage constant.

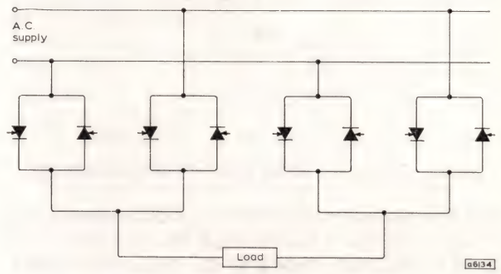


Fig. 45—Single-phase cyclo-converter

Cyclo-converter

The cyclo-converter is probably the simplest means of providing variable frequency, but it suffers from the disadvantage that without resorting to multiphase supplies the output frequency is normally limited to one third of that of the supply. A single-phase cyclo-converter power circuit is shown in Fig. 45. On a multiphase system (Ref. 4) a large number of thyristors are required. The advantage of the cyclo-converter is the ease with which the output voltage waveform can be made near-sinusoidal, especially at low frequencies.

Sequential Switching

Sequential switching provides an action similar to that of the commutator of a d.c. machine. The currents are switched in sequence round the field windings of the machine, thereby producing a rotating field. Although

one advantage of this system is that regeneration is easily achieved, and its operation is quite simple, it does however require more thyristors than the systems described previously.

PRACTICAL CIRCUIT

The circuit diagram of the complete two-phase motor control system is shown in Fig. 50.

COMPARISON OF SYSTEMS

It has been shown that a two-phase a.c. motor control system is technically possible and costs less than an equivalent three-phase system.

At present day prices the thyristors constitute the major part of the component cost, therefore the two-phase method of inversion offers a considerable price advantage over the equivalent three-phase system. The two-phase inverters use four thyristors and the three-phase bridge inverter uses a minimum of eight. However, this cannot be used as a direct comparison of the relative costs because owing to the poor couplings between the two halves of the motor windings on the two-phase inverters, the thyristor voltages are three to four times that of the supply, and so reduced supply and motor voltages are necessary. This means that although fewer thyristors are used they have to be of a higher current rating for the same horsepower system and of the same order of voltage. For a 1hp system the cost of thyristors for a three-phase bridge inverter is approximately 50% greater than that for the two-phase system.

Comparing the estimated cost of the two-phase system with that of an equivalent d.c. motor control system gives a factor of only 1½ to 2 times that of the d.c., when the differences in motor costs are taken into account. Though the a.c. motor control system is more expensive, the advantages of using squirrel cage induction motors make the two-phase a.c. motor control system a more practical proposition.

In performance, the two-phase system is not ideal on three counts:

(i) Because of poor coupling between the two halves of each motor winding the voltages in each inverter are three to four times that of the supply and so a reduced supply voltage is necessary.

(ii) With centre tapped stator windings each half carries the full current for half the time, so the stator losses are twice those of a single winding, therefore if the stator and rotor losses are equal the overall losses are about 50% greater because of this.

(iii) The motor voltages as supplied by the inverters have square waveforms. The harmonics of the square wave produce a slight decrease in efficiency, and the sequential switching on the stator produces a pulsating torque at low speeds. This pulsating torque becomes significant at speeds below 200 rev/min.

It should be noted that the disadvantages occur only in the method of inversion. It is therefore recommended that the two-phase system be used where low cost is the governing factor. When higher efficiencies and wider speed ranges are required, the three-phase inverter system should be used.

The control system described in this article is suitable for both two- and three-phase inverters with additional stages added to the ring counter for three-phase.

The performance figures for the two-phase system are given in Appendix 2. They show that the regulation at any speed is very nearly equal to that of the machine on a normal 50Hz supply. The frequency limit by current greatly improves the starting and overload characteristics. Measurements show that the acceleration rate is doubled.

It is considered that, for efficiency and performance reasons, a reasonable limit on power for the two-phase control system is about 5hp. For higher powers, where cost is not of prime importance, it is expected that three-phase inversion methods will give better performances and will therefore have wider applications.

A possible solution to the inverter voltage problem is given in Appendix 3. This is an initial investigation into using inverters in series to allow higher d.c. supply voltages to be used. The two-phase system was modified to connect the two inverters in series, and from the first tests there seems to be no reason why this method of operation should not be adopted.

APPENDIX 1

Effect of Rotor Power Factor on Torque

The two-phase squirrel cage induction motor may be represented as shown in Fig. 46. If there are alternating stator fields in the direction of Φ_1 and Φ_2, which are quadrature, in both space and time relationships, then the rotor induced e.m.f.'s are at a maximum when the rate of cutting flux is highest and are therefore in vector phase with the flux paths.

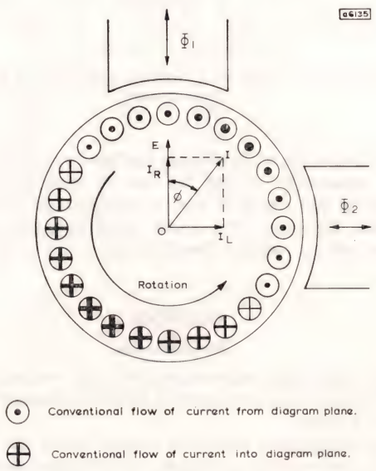


Fig. 46—Current distribution in the rotor of a two-phase squirrel cage motor

Let Φ_1 be a maximum, then the rotor voltage is as shown by the vector OE. Because the rotor circuit is inductive as well as resistive, the rotor current lags the voltage by an angle determined by the cosine of the ratio between the rotor resistance and its impedance as shown on the impedance triangle in Fig. 47. In other words, $\cos\phi$ is the power factor of the rotor.

The force on the conductors carrying the rotor current is at right angles to the flux Φ_1, so the component of I in phase with the flux is Icosϕ. The force is therefore given by BℓIcosϕ for each conductor, where ℓ is the length of the conductor.

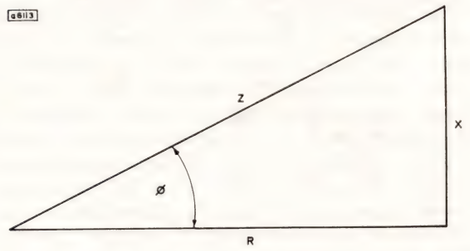


Fig. 47—Impedance triangle

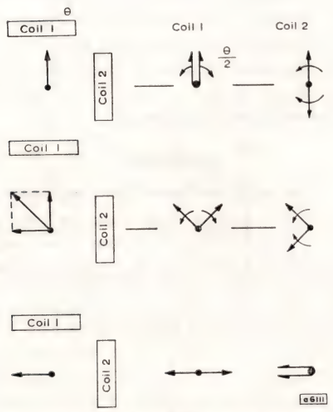


Fig. 48—Development of a rotating field from a two-phase field system

The generation of the rotating field can be shown by vectors. Each sinusoidally varying flux can be represented by two vectors of half the peak flux in magnitude and rotating in opposite directions. The phase relationships between the vectors and the resultant fluxes are shown in Fig. 48.

APPENDIX 2

Measurements

The work and measurements on the two-phase motor control system were performed on the motor supplied by Brook Motors Limited.

The torque-speed curves for various speeds are shown in Fig. 49, from which it can be seen that the characteristics of the motor when used on the variable frequency system are very nearly the same as those for the motor when connected to a fixed supply. The regulation at maximum speed (1500 rev/min) between no load and full load is about 4%. The actual fall in speed with load is approximately constant and independent of set speed.

Measurements of efficiency of the overall system showed the approximate value to be between 50 and 60%. Most of the losses were in the motor. As stated in *Comparison of Systems*

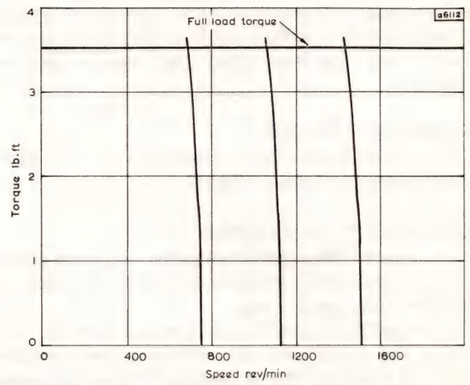


Fig. 49—Torque-speed characteristics of a two-phase system

(page 233), nothing has yet been done to optimise the design of the motor windings. It may mean that a slightly larger frame size for the motor will be necessary to minimise the copper losses.

APPENDIX 3

Series Operation of Inverters for Motor Control

Owing to high voltage development in the inverter circuits, it was decided to connect the inverters of the two-phase system in series. This was to make it possible to run the system from a 415V three-phase a.c. supply without a transformer.

The present system with the inverters in parallel is limited to a d.c. supply of about 250V because this gives 750 to 1000V across the thyristors. With the inverters in series, the d.c. supply voltage can be doubled.

When connected to a 415V three-phase supply with the thyristors fully conducting, the d.c. output voltage would be 562V. A 250V motor could be used if phasing back were used to give a d.c. voltage of 500V, which would allow for regulation under load.

Apart from connecting the inverters in series, the only other major modification which seems to be necessary is for the smoothing capacitor to be connected across each inverter and not across the d.c. supply. This is required for two reasons. Firstly, it splits the d.c. supply voltage so that the inverters can start operating, otherwise one inverter has to be working before the other can start, unless square waves are used for triggering. Secondly, the inductive energy in the inverters and loads must be fed back into a low impedance supply, and without the two capacitors this energy can only be fed back via an inverter circuit.

There is one minor difficulty to be overcome with series operation of inverters. The current through the inverters falls to zero during the thyristor conduction period, consequently the particular thyristor conducting at that time turns off. In the two-phase motor control circuit, the thyristors are triggered from relatively narrow pulses so that when a thyristor turns off it cannot be turned on again until the next cycle. This is not considered to be a serious objection to using thyristor inverters in series. The problem has been overcome temporarily by cross coupling the anodes and gates of the two thyristors in each inverter with resistors and connecting voltage regulating diodes between the gates and cathodes. The trouble with this is that the power dissipation in the resistors is rather large at high inverter voltages.

The series operation of inverters for a.c. motor control is to be investigated further.

COPY OF TEST CERTIFICATE

TABLE 1

Motor tests on sinusoidal waveform supply

Data:

Sync Speed: 1500		Phase	: 3	Volts	: 220/240, 380/420
Frame	: D162/4R	H.P.	: 1·0	Rotor	: Cage
Poles	: 4	Rating	: C.M.R.	Frequency	: 50Hz
		Type	: T.E.F.C.		

All tests on 230V r.m.s. supply

Performance Test

B.H.P.	Amps.	Kilowatts			Speed	Slip %	Power Factor		Eff %
		W1	W2	W1+W2			1	2	
No Load	2·12	·335	—·17	·165	1500				
·561	2·3	·5	·1	·6	1470	2·0	·66	·665	69·7
·706	2·7	·58	·16	·74	1450	3·33	·69	·71	71·1
·974	3·16	·7	·29	·99	1430	4·66	·77	·79	73·6
1·178	3·7	·83	·38	1·21	1400	6·68	·822	·84	72·6

Temperature Test (stray losses deducted)

Time	Amps.	Kilowatts			Speed	Temperature °C	
		W1	W2	W1+W2		Room	Frame
12·00	3·16	·7	·29	·99	1430	22	—
1·00	3·16	·7	·29	·99	1420	24	39
2·00	3·14	·7	·29	·99	1420	25	40
3·00	3·14	·7	·29	·99	1420	25	41
—		After a period standing				—	46

Final temperature rise: frame, 21°C, winding, 45·5°C

Starting Torque (By resistance)

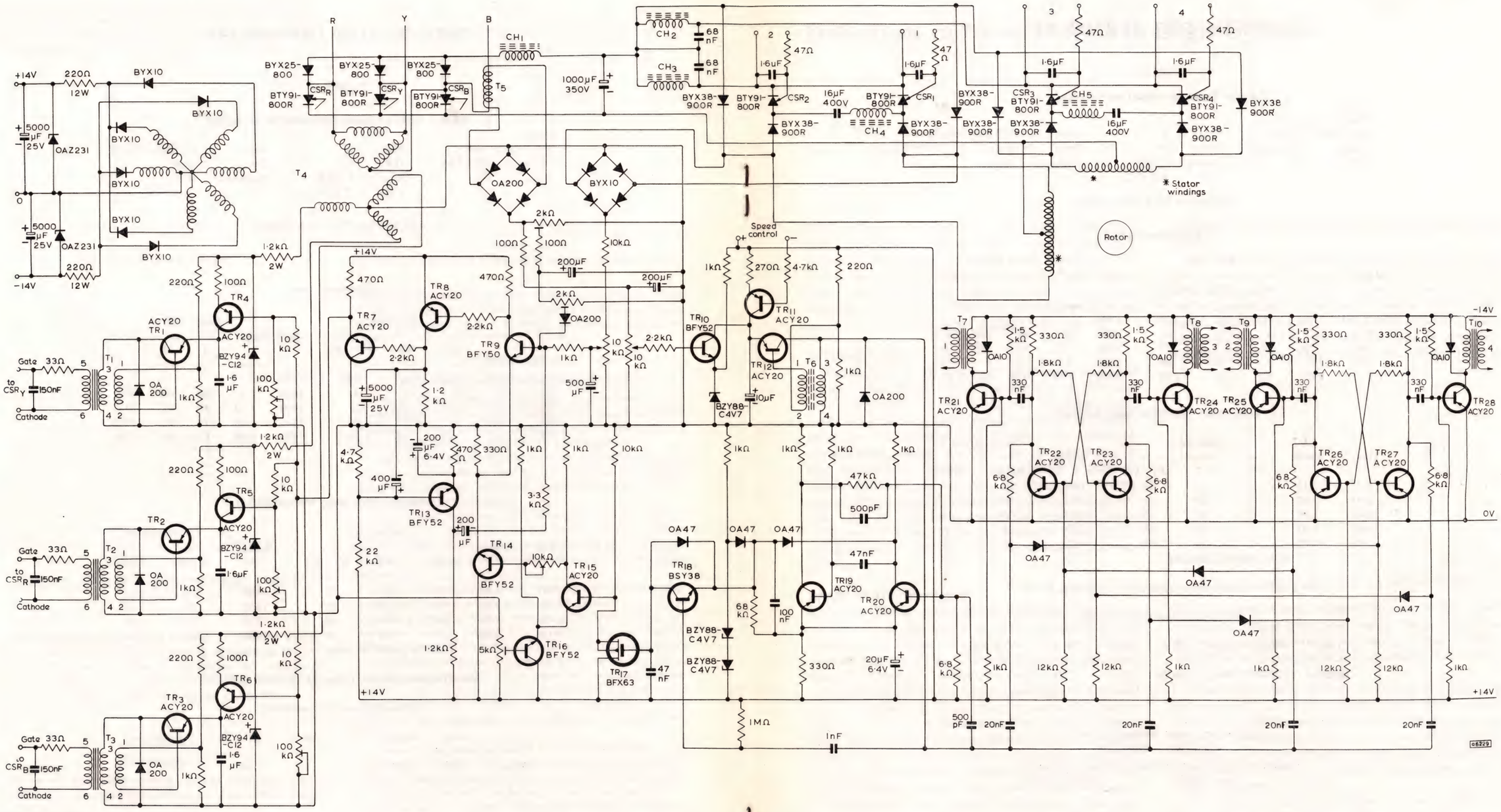
Conn.	Volts	Amps	KW	Lb.ft.	%F.L.T.	%F.L.C.
Delta	228	15·85		8·5	243	

Equivalent stator resistance (ohms):
Cold: 10·1, Hot: 12·0

Flash test (volts for one minute), Insulation resistance,
stator: 2000. stator: 50MΩ.

Table 2, for square-wave supply, is on page 238.

SPEED CONTROL OF TWO-PHASE A.C. INDUCTION MOTORS



TRANSFORMER AND CHOKE DETAILS

T_1–T_3 Core, FX2239 1 pair each with bobbins.
Windings 1, 2: 160 turns 40 s.w.g. en. cu.
3, 4: 80 turns 34 s.w.g. en. cu.
5, 6: 80 turns 34 s.w.g. en. cu.
Insulation on winding 5, 6 to withstand three-phase supply peak voltage.

T_4 Primary to suit supply.
Secondary 1: 30V 100mA per phase.
Secondary 2: 50–0–50V 200mA per phase.

T_5 Core, English Electric Z371038.
Winding: 2500 turns 40 s.w.g. en. cu.

T_6 Core, FX2239 1 pair with bobbin.
Winding 1, 2: 160 turns 40 s.w.g. en. cu.
3, 4: 80 turns 34 s.w.g. en. cu.

T_7–T_{10} Core, FX2238 1 pair each with bobbins.
Winding 1: 210 turns 34 s.w.g. en. cu.
2: 210 turns 34 s.w.g. en. cu.
Insulation to withstand 1000V.

CH_1 Core, English Electric Z371001 2 pairs.
Winding: 20 turns 10 s.w.g. en. cu.

CH_2–CH_3 Core, English Electric Z371003 2 pairs each.
Winding: 154 turns 14 s.w.g. en. cu.

CH_4–CH_5 Core, FX2239 1 pair with bobbin.
Winding: 6 turns 18 s.w.g. en. cu.

The OA10 is being superseded by the BAX78.

Fig. 50—Two-phase a.c. motor control system

COPY OF TEST CERTIFICATE

TABLE 2

Motor Tests on square-wave supply

Data:

Sync Speed	: 1500	Phase	: 3	Volts	: 220/240, 380/420
Frame	: D162/4R	H.P.	: 1·0	Rotor	: Cage
Poles	: 4	Rating	: C.M.R.	Frequency	: 50Hz
		Type	: T.E.F.C.		

All tests on 230V r.m.s. supply

Performance Test

B.H.P.	Amps.	Kilowatts			Speed	Slip %	Power Factor		Eff %
		W1	W2	W1+W2			1	2	
No Load	2·0	·285	−·12	·165	1500				
·552	2·28	·5	·1	·6	1470	2·0	·66	·665	68·6
·694	2·58	·56	·17	·73	1450	3·33	·714	·732	70·9
·958	3·15	·7	·28	·98	1430	4·66	·783	·8	72·8
1·2	3·68	·83	·4	1·23	1400	6·68	·838	·852	72·7

Temperature Test (stray losses deducted)

Time	Amps.	Kilowatts			Speed	Temperature °C	
		W1	W2	W1+W2		Room	Frame
8·45	3·15	·7	·28	·98	1430	18	—
9·45	3·07	·7	·28	·98	1420	20	34
10·45	3·07	·7	·28	·98	1420	20	35
11·45	3·07	·7	·28	·98	1420	21	36
1·00	3·07	·7	·28	·98	1420	23	38
—	After a period standing				—		44

Final temperature rise: frame, 20°C, winding, 45·5°C

Starting Torque (By resistance)

Conn.	Volts	Amps	KW	Lb.ft.	%F.L.T.	%F.L.C.
Delta	230	14·8	5Ω/3P	8·0	228	

Equivalent stator resistance (ohms):
Cold: 10·1, Hot: 12·0

Flash test (volts for one minute), Insulation resistance,
stator: 2000. stator: 50MΩ.

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ACKNOWLEDGEMENT

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Definitions of Noise Margin in Logic Systems

C. F. HILL
Mullard Central Application Laboratory

This article provides a definition of the 'noise margin' of a device: the definition is in a form which facilitates the estimation of the overall performance of a system using the device, when spurious signals are applied. The definition allows easy comparisons between devices and provides circuit design information. The basis of the definition is the use of the input-versus-output transfer characteristic.

INTRODUCTION

The purpose of this article is to clarify the meaning of the term 'noise margin' when it is used with reference to a logic switching circuit within a system. An assessment is made of definitions in use at present; although the present definitions are adequate for devices with particular characteristics, reasons are given for the inadequacy of such definitions in the general case. Finally a definition is given that allows an easy means of comparison between devices, provides useful design information and is compatible with the test requirements for mass production techniques. It is thought that this definition could lead to standardisation in the use of the terms relating to noise margin.

BASIC LOGIC SYSTEMS

In a computing system, decision signals are taken from bistable circuits and passed, via chains of gate circuits, to the inputs of further bistable circuits. A simple block diagram is shown in Fig. 1. The bistable circuits themselves may well consist of cross-coupled gates.

In such a system, noise voltage signals may be produced at various inputs (Fig. 1) by voltage or current disturbances internal or external to the system. The maximum value of these noise signals before the system behaves incorrectly is termed 'noise margin'. This term is applied to the gate circuit and its value may depend on whether the noise signal is applied to one or more gates within the system.

In this article distinction is made between the 'noise margin voltage' and 'noise immunity', terms which have sometimes been used synonymously. As stated above, noise margin is the property of the circuit to withstand unwanted signals at its input, and should not take into account the likelihood of such unwanted signals being produced. It would be useful if the noise immunity of a system were defined as the likelihood of spurious signals being generated when the circuit is used in a system. As such, noise immunity may be given as a figure of merit which would include factors such as noise margin. Noise immunity, however, is not discussed in detail in this article.

The meaning of incorrect behaviour of the system can be considered with reference to Fig. 1. As shown, noise signals can be applied to inputs of all gates including the bistable circuit; the amplitude and polarity of these signals could be unique to the particular system. Equal noise signals on all inputs, for example, may arise from disturbances on the supply lines or earth lines. In more fully integrated circuits, the inputs exposed to the 'outside world' may receive larger noise signals than those internal to the package. The polarity of the noise voltages, however, may differ for the various inputs, depending on such things as the interconnection pattern.

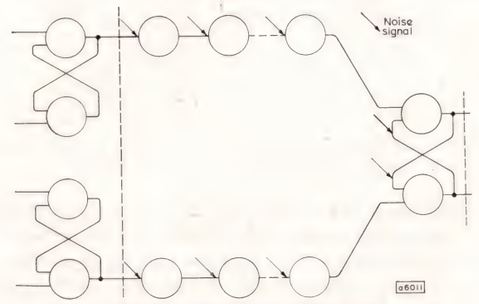


Fig. 1—Chain of gates driving a bistable circuit

The noise signals on the cascaded gates will affect the input voltages to the bistable circuit. This situation will prove troublesome if the input signal voltage, plus the noise voltage at the input, causes the bistable circuit to change to its alternative stable state. The bistable circuit may also be incorrectly switched by noise signals on the cross coupled inputs alone.

It is worth noting that the gates themselves effectively have no memory; that is, on removal of the noise signals the gates will return to the logic states existing before the disturbances, provided, of course, that no new information has been fed into the chain, such as would occur if one of the previous bistable circuits in the system had switched over.

CHARACTERISTICS OF SINGLE GATES

The effect of noise signals on gate circuits can be determined by a study of their transfer characteristics,

these being plots of input voltage against output voltage. Fig. 2a shows the transfer characteristic of an AND or OR (non-inverting) gate, and Fig. 2b shows the transfer characteristic of a NAND or NOR (inverting) gate. Swinging the input level through the transfer region causes the output to switch from one logic level to the other.

Fig. 3 shows an idealised characteristic for an inverting gate; the input to such a gate will be at point A or B given by the output of a previous stage. Ideally, the transfer

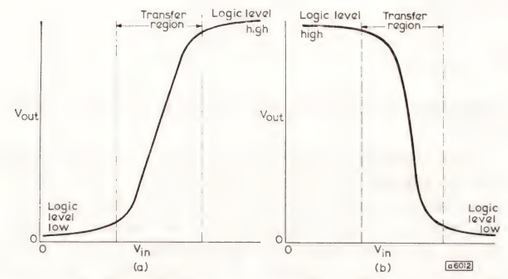


Fig. 2—Transfer characteristics of non-inverting and inverting gates

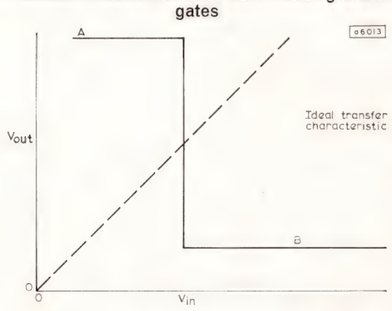


Fig. 3—Ideal transfer characteristics

region will be midway between A and B, and in such a case, the definition of noise margin would be simple; it would be the input voltage difference between that given by the transfer region and that given by point A or point B. The circuit can tolerate this amount of input without actually switching.

The first move away from the ideal is when points A and B are no longer equidistant from the transfer region; under these conditions, the switching voltage will depend on whether the input is at A or at B. This situation will give two values of noise margin.

A further deviation from the ideal occurs when the transfer region takes up a finite slope and there is a rounding-off of the logic levels, as was seen in Figs. 2a and 2b. The question then arises as to what the noise margin is, relative to points A and B. One approach is to take a point midway along the transfer region, and to measure the input voltage swings to this point from A or B. However, it will be shown that this has limited validity with respect to the signals that can be applied to the circuit, when it is in a system, without incorrect behaviour of the system.

Another approach is to take arbitrary points along the characteristics and assume or hope that the measure of the permissible unwanted signals given by these points will not give rise to incorrect behaviour. These arbitrary points are sometimes given as a percentage of the logic swing away from points A or B, or sometimes as the points where the slope of the characteristic is unity. It so happens that the majority of circuits to date have little rounding-off

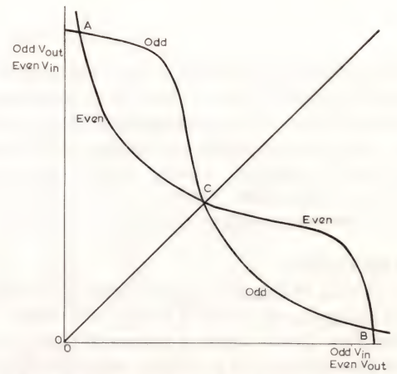


Fig. 4—Transfer characteristics for a chain of inverting gates

of the logic levels, and the transfer region is very steep compared with the logic swing; as a consequence the above arbitrary points, as will be shown, give a safe if somewhat pessimistic figure for noise margins.

CHARACTERISTICS OF A CHAIN OF GATES

Consideration can now be given to a chain of gates, as given in Fig. 4. Assume this chain to be of infinite length and made up of identical gates, such as NAND or NOR gates. The transfer characteristics of the individual gates will be of the type shown in Fig. 2b; the outputs of the odd stages will be the inputs to the even stages, and vice versa. The transfer characteristics of the odd and even stages can be plotted on the same axes, as shown in Fig. 4; the characteristic for the even stages can be obtained by rotation of the odd characteristic about the axis of unity slope (45°) through the origin.

If the input to the first stage is 0V, then within a few stages the output voltages will be given by the operating point A, if we assume the absence of noise signals. By using a 'zig-zagging' procedure from one transfer characteristic to the other in Fig. 5 (which is an expanded and exaggerated form of the upper loop shown in Fig. 4) it can be seen that the point A is reached within six stages. Again, if the signal input to the first stage is only slightly less than the voltage given by the operating point C, then, in the absence of noise signals, the operating point A will be reached within a few logic stages; Fig. 6 shows nine stages. A similar approach for a voltage slightly greater than that given by the operating point C, shows that the operating point B is reached, in the same way, in the absence of noise signals (Fig. 7).

It follows that for an infinite chain, the outputs of all stages, in the absence of noise signals, will be given by either operating point A or operating point B, shown in Fig. 4. (In the above example, a chain of more than nine stages represents a quasi-infinite chain of gates, and can be treated as infinite). Point A gives a high level output for the odd stages, and a low level output for the even stages, and the reverse is true of point B.

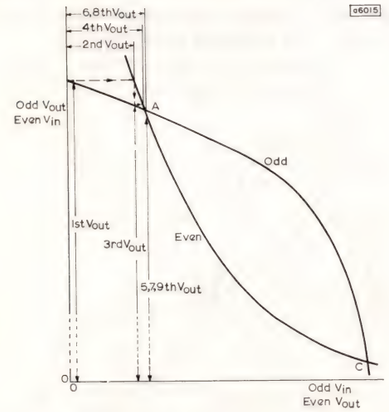


Fig. 5—Output voltages for a chain of inverting gates when $V_{in} = 0V$ and no noise voltages are applied

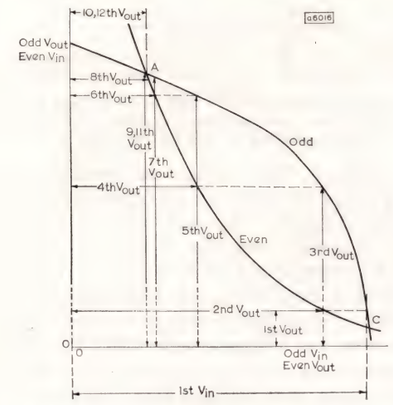


Fig. 6—Output voltages for a chain of inverting gates when $V_{in} < V_c$ and no noise voltages are applied

A degree of familiarity with the above zig-zagging procedure between characteristics will be an advantage to the reader in the discussions that follow.

INTRINSIC NOISE MARGIN OF A SINGLE CIRCUIT

Assume that the outputs are given by the operating point A shown in Fig. 4, and that a positive noise signal N_1 is applied to the input of an odd stage, say stage 1. Assume also that no other noise signal is present. If the input voltage (on the odd characteristic) to the first stage ($V_A + N_1$) is less than the voltage given by the operating point C then, as stated above, and as is evident from Fig. 6, the outputs of stages 9, 10, 11, 12 etc., will be given by point A, even though the noise signal is still present on the input of stage 1. If now N_1 is made to take the input of the first stage to the operating point C, then the output of stage 1 and all the succeeding stages will be given (unstably) by point C, during the time that N_1 is present. Again, if N_1 takes the input of stage 1 to a voltage greater than that given by point C, then, from previous discussions and from Fig. 7 it is evident that the outputs of stages 9, 10, 11, 12 etc., will be given by point B during the time that N_1 is present.

Points A and B can be seen to be stable equilibrium

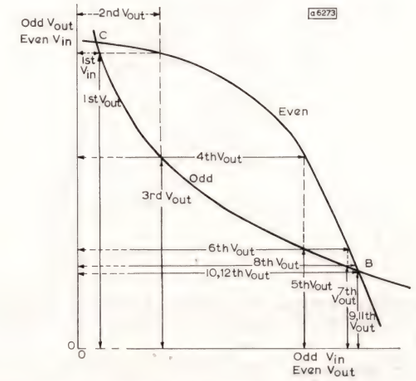


Fig. 7—Output voltages for a chain of inverting gates when $V_{in} > V_c$ and no noise voltages are applied

points, whilst C is an unstable equilibrium point. Similar arguments can be considered if a negative noise signal N_2 is applied to an even stage and it is assumed that there are no other noise signals. The cross-over point C plays an important role in defining the intrinsic noise margin; the definition will be finalised below. For the present, this definition can be taken as that voltage which will take the input from the voltage given by the particular logic state to that given by the cross-over point (C) of the superimposed characteristics.

There will be a value for intrinsic noise margin for each of the logic states. For nominal curves, the cross-over point falls on the axis of unity slope through the origin where $V_{in} = V_{out}$. However, when spreads in characteristics are considered, the cross-over point no longer occurs at the point $V_{in} = V_{out}$; this matter will be discussed later.

WORST CASE NOISE MARGIN FOR A CHAIN OF GATES

Consideration is now given to the case in which noise signals are applied to more than one gate in the chain of inverting NAND or NOR gates. Let the odd outputs be at the high level, and the even outputs at the low level; this condition is given by the point A of Fig. 8, which is the expanded loop of Fig. 4. Assume the noise signals N_1, N_3, N_5, etc., applied to the odd stage inputs, are positive, and that N_2, N_4, N_6, etc., applied to the even stages are negative.

If we use the zig-zag procedure between characteristics,

we see that the stage outputs are given by operating points 1, 2, 3, etc. From the discussions on the intrinsic noise margin, the following point holds: if a noise signal takes the output of a particular stage to a voltage less than, equal to, or greater than, the voltage given by point C, and if there are no noise signals on the succeeding stages, then the input and output of these stages will be given by the points A, C or B respectively.

Suppose now that the odd stages each receive a noise

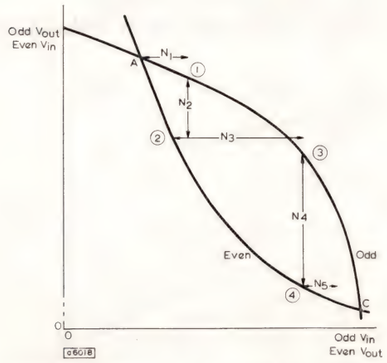


Fig. 8—Output voltages for a chain of inverting gates when noise voltages N_1, N_2, N_3, etc. are applied to inputs 1, 2, 3, etc.

signal of amplitude $+N_P$ and that there are no noise signals on the even stages, then the following equations apply.

$$V_{in(odd)} = V_{out(even)} + N_P$$
$$V_{in(even)} = V_{out(odd)} .$$

Then the input and output of the odd stages will be given by the point 1 in Fig. 9, and the input and output of even stages by point 2. If the amplitude of N_P is greater than the maximum width of the loop along the odd V_{in} axis, then the output and input operating points will rapidly approach the point B, the operating points being 1 and 2 shown in the expanded axis of Fig. 9. Thus false information will be given to the final bistable circuit. (The requirements of the bistable circuit will be discussed later.) Therefore, $N_{P(max)}$ is given by the maximum width of the loop in the odd V_{in} direction.

A similar reasoning applies if a negative noise signal $-N_Q$ is applied to each of the even stages while there are no noise signals on the odd stages. Here N_Q maximum will be the maximum width of the loop in the even V_{in} direction. From the mirror symmetry of the curves it follows that

$$+N_{P(max)A} = +N_{Q(max)B}$$

and

$$-N_{Q(max)A} = -N_{P(max)B} .$$

Alternative Graphical Procedure

An alternative graphical approach to noise margin is as follows. Assume N_P is the positive noise signal on the odd stages and that $N_Q = 0$; then, as stated before, the input and output voltages will be given by the operating points 1 and 2 in Fig. 9. If the odd characteristic is shifted horizontally to the left by an amount N_P, then points 1 and 2 become coincident, becoming, in effect, the new position of cross-over instead of point A.

As N_P is increased, the modified cross-over points, A and C, approach each other, and become coincident when $N_P = N_{P(max)}$. Any further increase in N_P shifts the odd curve still farther to the left and the only remaining cross-over point is B, indicating a switch over of states.

Consideration can now be given to the conditions where there is a positive noise signal $+N_P$ on each of the odd stages, and a negative noise signal $-N_Q$ on each of the even stages. The following equations apply.

$$V_{in(odd)} = V_{out(even)} + N_P$$
$$V_{in(even)} = V_{out(odd)} - N_Q .$$

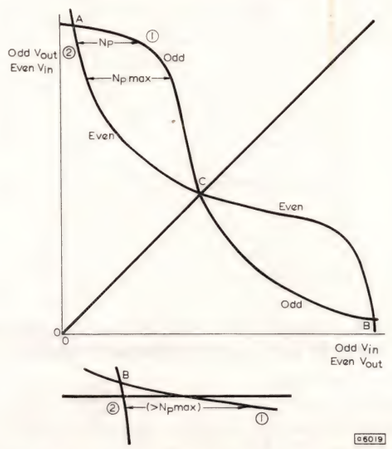


Fig. 9—Transfer characteristics with noise voltage N_P applied to odd stages only, giving operating point 1 for odd stages and operating point 2 for even stages

If in addition, $|N_P| = |N_Q|$, the operating points 1 and 2, as shown in Fig. 10, are the diagonal corner points of a square of side N_P. The maximum noise signal in this situation is given by the side of the maximum square that can be drawn within the loop. As before, a positive noise signal to each of the odd stages can be depicted graphically by a horizontal shift to the left of the odd characteristics, and a negative noise signal to each of the even characteristics can be depicted by a vertical shift upwards of the even characteristics; hence the points 1 and 2 of Fig. 10 become coincident if one characteristic is fixed and the other shifted along the axis of unity slope through the origin. As $|N_P|$ and $|N_Q|$ are increased, then, as before, A and C become coincident, giving the maximum noise signal. If the noise signals are increased beyond $N_{P(max)}$, then the equilibrium situation will be as in the expanded axis of Fig. 10, this being an extension of the characteristics beyond the cross-over point B.

The maximum square in the loop is the graphical representation of a worst case noise margin, which could be defined as follows. In the absence of any noise signals, the outputs in an infinite chain of gates will be in well defined states and if a noise signal voltage is applied adversely to all the inputs, then when the signal is increased all the odd outputs will increase in unison, as will the even outputs: the worst case noise margin is that

voltage which will cause all outputs to suddenly take up their complementary states.

It is worth noting, that the quasi-infinite chain we have considered so far, has, in practice, a beginning or first stage; as a consequence, despite the above definition, when the noise voltage is removed the gates will revert to their original states. If, however, a genuinely infinite

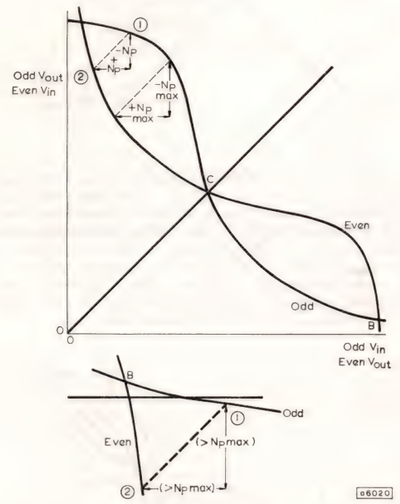


Fig. 10—Transfer characteristics with noise voltage $+N_P$ applied to all odd stage inputs and $-N_P$ applied to all even stage inputs

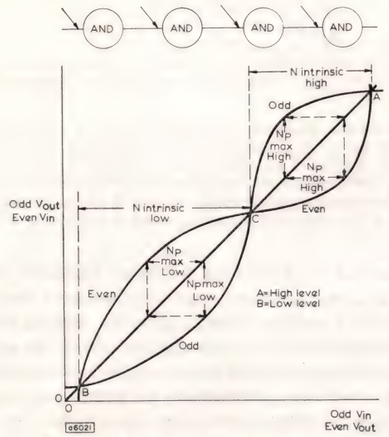
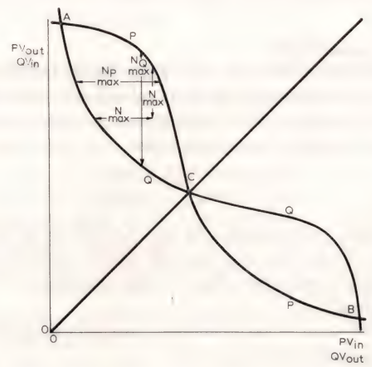


Fig. 11—Transfer characteristics for a chain of non-inverting gates. $N_{intrinsic\ (low)}$ is positive and $N_{intrinsic\ (high)}$ is negative and both can be applied to one stage only. $N_{P(max)\ low}$ is positive and $N_{P(max)\ high}$ is negative and both can be applied to all stages

chain of gates with no beginning or end is considered, then on removal of the noise signal the gates will not revert to their original states. This point is further emphasised when discussing bistable circuits which act as ideal infinite chains without beginning or end.

NON-INVERTING GATES

So far, only inverting gates have been discussed; however, similar arguments will hold for non-inverting gates. Fig. 11 gives the characteristics and the block diagram for a chain of AND or OR gates. As before, the odd and even characteristics can be obtained by rotating either of them about the axis of unity slope through the origin. Although the loops of the characteristics are symmetrical in themselves about this axis, there is no symmetry between the two loops.



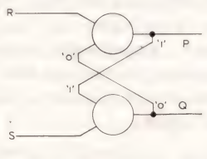


Fig. 12—Transfer characteristics for a bistable circuit consisting of cross-coupled NAND gates. Noise is applied to cross-coupled inputs only. N_P relates to the P gate only, N_Q to the Q gate only, and N to both gates

The point C is used in the definition of intrinsic noise, and, as before, there will be two values of intrinsic noise margin, one for positive noise and the other for negative noise. Adverse noise signals for odd and even stages will be of the same polarity. If equal adverse noise signals are applied to all gates and the amplitude is increased, there will come a point where the outputs will be seen to have changed states. This worst case noise margin will be given by the side of the maximum square capable of being drawn within the loops. Because of the asymmetry of the loops with respect to each other, there will be two values for worst case noise margin.

CHARACTERISTICS OF BISTABLE CIRCUITS

Fig. 12 gives the block schematic diagram and transfer characteristics for a cross-coupled NAND or NOR circuit. R and S are reset and set inputs; R and S are normally at '1' for the cross-coupled NAND gate, and they will normally be at '0' for the cross-coupled NOR gate.

The characteristics are drawn such that

$$V_{in(P)} = V_{out(Q)}$$
$$V_{in(Q)} = V_{out(P)} .$$

As previously described, they are obtained one from the other by rotation about the axis of unity slope through the origin.

A trivial bistable circuit can be obtained by cross-coupled AND or OR gates. The solution is trivial on two counts, firstly, the outputs are both '0', or are both '1', and secondly, set and reset control cannot be used.

NOISE MARGIN OF BISTABLE CIRCUITS

Noise margin for the cross-coupled inputs or the set-reset inputs can be discussed with reference to Fig. 12.

Cross-Coupled Inputs

If we ignore the set and reset inputs, the bistable circuit can be treated as an idealised infinite chain without a first or last stage. If N_P and N_Q are the noise signals on the P and Q gates respectively, then

$$V_{in(P)} = V_{out(Q)} + N_P$$
$$V_{in(Q)} = V_{out(P)} + N_Q.$$

For adverse noise signals, N_P and N_Q will be of opposite polarity. From the previous discussion concerning an infinite chain, and from Fig. 12, the following statements can be made.

(i) The state of the bistable circuit will be defined by operating point A or B.

(ii) If applied to the low input stage only, or to the high input stage only, the maximum adverse noise voltage is given by the maximum width of the loop along the relevant input axis. Adverse noise voltage is positive for low input stages, negative for high input stages.

(iii) If equal amplitude noise voltages are applied to both inputs, with positive noise applied to the low input, and negative to the high, then the maximum adverse noise signal is that voltage given by the side of the maximum square within the loop.

(iv) If adverse noise signals greater than those defined above are applied, then the bistable circuit will switch to its complementary state. (See Figs. 9 and 10).

Set and Reset Inputs

In a bistable consisting of cross-coupled NAND gates, Fig. 12, R and S will normally be at '1'. Assume noise voltages are applied to R and S but not to the cross-coupled inputs, then it may be shown that the bistable can only be affected by negative noise to the input of the gate whose output is low; in the circuit shown, this means a negative voltage on S, the output of Q being low. The outputs of P and Q will be determined by the negative voltage on S provided the operating point C is not reached. If, however, the operating point C is reached, an unstable equilibrium is achieved. If the negative voltage on S is further increased beyond C, then the cross-coupled inputs will take control and the bistable will rapidly switch to its complementary state. Therefore, for the set and reset inputs the maximum adverse noise signal is given by the negative intrinsic noise margin previously discussed.

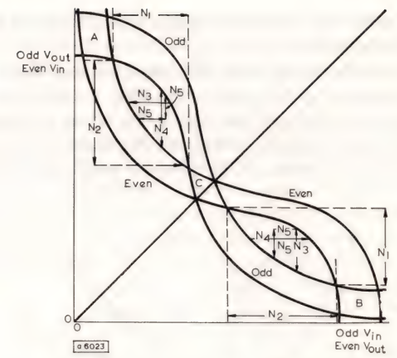


Fig. 13—Noise margins when applied to the system shown in Fig. 1. N_1 and N_2 represent intrinsic noise margins: N_1 is the maximum positive noise when applied to one low input, and N_2 is the maximum negative noise when applied to one high input, but neither of these relate to cross-coupled inputs. N_3 is the maximum positive noise if applied to all low inputs, and N_4 is the maximum negative noise if applied to all high inputs. Worst-case noise is represented by N_5, the maximum when applied to all inputs adversely.

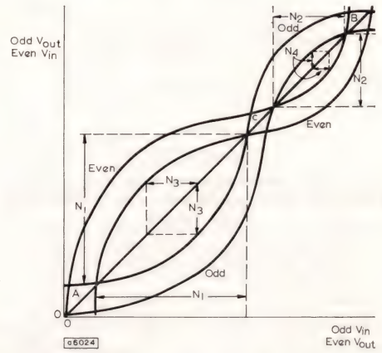


Fig. 14—Noise margins when applied to a chain of non-inverting gates. N_1, and N_2 indicate intrinsic noise margin: N_1 is the maximum positive noise if applied to one low input, and N_2 is the maximum negative noise if applied to one high input. N_3 is the maximum positive noise if applied to all inputs, and N_4 is the maximum negative noise if applied to all inputs

SPREADS IN TRANSFER CHARACTERISTICS

So far, only nominal characteristics have been considered; in a practical system, however, spreads will also need to be considered. These spreads will be the result of environmental conditions such as supply voltage variation, loading variation, temperature variation, and also the result of production spreads for the devices. The result will be an envelope containing the full spread of transfer characteristics of the form shown in Fig. 13 which is for inverting NAND or NOR gates.

If we now wish to consider the various noise margins within a part of a system consisting of a chain of gates followed by a bistable circuit, the relevant characteristics are obtained by rotating the envelope of Fig. 13 about the axis of unity slope through the origin. From the restricted loops of Fig. 13 and from the foregoing discussion, the following points can be stated.

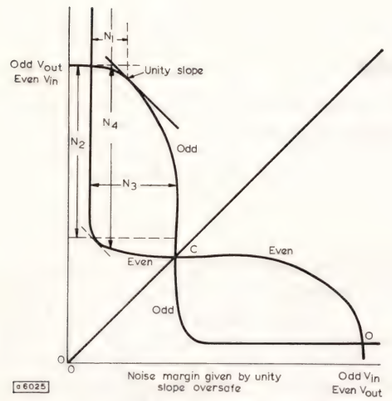


Fig. 15—Noise margin as given by the unity slope method is over-safe with the transfer characteristic shown

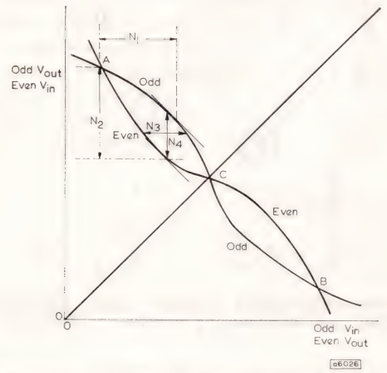


Fig. 16—Noise margin as given by the unity slope method is under-safe with the transfer characteristic shown

(i) If a noise signal is applied to one input only in the chain, then the maximum adverse noise is given by N_1 or N_2 in Fig. 13 depending on the input state. This holds also for the set and reset inputs of the bistable, but not for the cross-coupled inputs. This noise margin is known as an intrinsic noise margin.

(ii) If a noise signal is applied to alternate gates in the chain, the maximum adverse noise is given by N_3 or N_4 in Fig. 13. This is true for the bistable circuit if the noise signal is applied to either one or the other of the cross-coupled inputs.

(iii) If adverse noise signals are applied to all inputs, the maximum value is given by N_5, the side of the maximum square within the loop in Fig. 13. This voltage is known as the worst case noise margin.

(iv) If AND or OR circuits are used in the chain, but not for the bistable circuit, then the noise margin values are given in Fig. 14.

ALTERNATIVE DEFINITIONS

Mention was made earlier (page 240) of the use of arbitrary points with which to measure noise margin; examples quoted were points of unity slope, or a percentage of the logic swing. Fig. 15 using the point of unity slope gives a cautious value when a positive signal is applied to the low inputs, or a negative signal is applied to the high inputs. Fig. 16 gives an unsafe figure if a positive signal is applied to the low inputs or a negative signal is applied to the high inputs.

PREFERRED DEFINITIONS OF NOISE MARGIN

The effect of noise voltage in a system has been discussed: the system considered has been a bistable circuit with inputs fed from chains of similar circuits. If similar gates (NAND or NOR) are used both in the chains and in the bistable, a definition of noise margin can be evolved relating performance in the system to the voltage transfer characteristics of the gates in the following way. If adverse noise is applied to all inputs, then a worst case noise margin is obtained which can be measured within the loops of the superimposed transfer characteristics as described in the text above.

This then gives rise to the following definition. In an infinite chain of gates the worst case noise margin is that voltage disturbance which can be applied simultaneously adversely to all inputs before the outputs switch to their complementary states. If AND or OR gates are used for the chain circuits, then the noise margin of the bistable circuit will have to be considered separately; in fact it is an idealised infinite chain in itself.

An intrinsic noise margin can also be defined by the superimposed transfer characteristics; essentially, it is the voltage swing between the stable and unstable equilibrium points. The intrinsic noise margin, together with the worst case noise margin, give a measure of the steepness of the transfer region.

It is considered that the use of the superimposed transfer characteristics will normally meet the requirements for comparisons between devices, for giving circuit design information, and for testing devices during production.

It is stressed that this article deals with the noise margins of circuits within systems, that is, the behaviour of the circuit and system, when subjected to unwanted signals being produced as a result of device and external circuit parameters. Ultimately, the design information required is probably a figure of merit combining these two factors. Such a figure of merit could be regarded as a definition of noise immunity. Noise immunity would therefore depend on such items as input and output impedances, peak currents and the noise margin value itself.

Transistor Field Timebases for Colour and Monochrome Receivers

B. E. ATTWOOD
Mullard Central Application Laboratory

A new type of scanning circuit with no field output inductor is described. It is suitable for scanning 90-degree colour picture tubes operating at 25kV, or 110-degree monochrome tubes at 20kV. The circuit operates in the class A mode, but one of the output transistors operates simultaneously as a driver and phase splitter for the other, thus simplifying the earlier stages of the timebase.

INTRODUCTION

Transistor timebase circuits usually operate in the class A mode with an output inductor which is relatively bulky and costly. Class B circuits have been fully investigated as an alternative approach, but although they provide a solution which avoids the use of an output inductor, they do not lend themselves to the easiest driving arrangements, and, in particular, are not as insensitive to component and transistor spreads as directly coupled class A circuits. Crossover distortion can also be a problem.

Directly coupled class A circuits of the type shown in Fig. 1 are particularly good in these respects because (a) the clamping action of the switch is carried through the

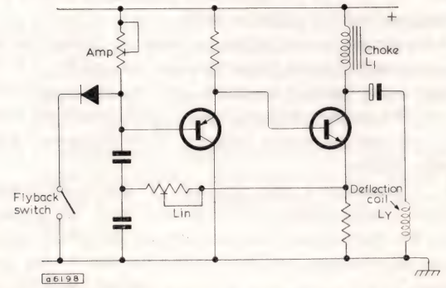


Fig. 1—Directly-coupled class A circuit (with output inductor) The 'flyback switch' may be a blocking oscillator multivibrator

circuit to the output device and (b) a simple emitter follower may be used to voltage-drive the output transistor, thus reducing the influence of current gain spreads.

Since it is desirable to achieve the performance of this type of class A circuit but without the choke, a further circuit has been developed in which a transistor replaces the choke. The advantages of class A operation are retained.

BASIC CIRCUIT

The basic operation of the circuit can be described with reference to Fig. 2. At the instant that flyback ends and scan begins (that is, as the switch is just opening), TR_3 is cut off since its base is at chassis potential, TR_2 being

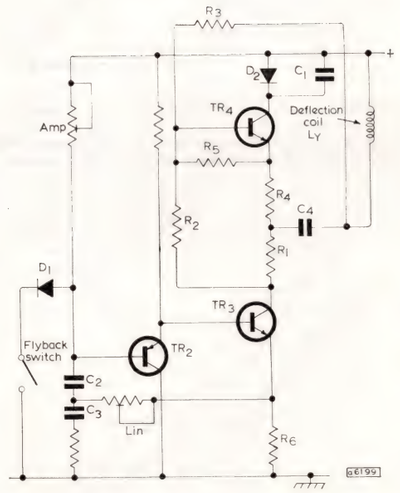


Fig. 2—Basic single-ended push-pull circuit. The 'flyback switch' may be a blocking oscillator multivibrator

bottomed by the action of the switch. Therefore no current will flow in either TR_3 or R_1. Approximately half the h.t. line voltage V_{ht} will be developed across C_4 (that is, the voltage across the deflection coil L_Y will swing about V_{ht} and the voltage at the emitter of TR_4 will swing about $\frac{1}{2}V_{ht}$). The base-emitter voltage of TR_4 will be, therefore, dependent primarily on the values of R_2, R_3, R_5, the input resistance of TR_4, and the effective battery voltage across C_4. The value of R_3 is chosen to ensure that TR_4 is conducting when TR_3 is cut off.

As the scanning stroke progresses, the current in TR_3 progressively increases, and a voltage develops across R_1. At the end of scan, the current through R_1 is such that the resultant voltage across it cancels the base-emitter voltage present at the base of TR_4 when TR_3 was 'off'. Thus, as the scan progresses, the current in TR_4 decreases while that in TR_3 increases.

During flyback, TR_3 is cut off, its base being clamped to chassis potential by the switch and the direct coupling through TR_2. As a result of the stored energy in the scanning coils, the voltage across L_Y rises positively, and takes the base and emitter of TR_4 positive. When the rising voltage reaches V_{ht}, diode D_2 will become non-conductive. The voltage across L_Y will then be free to rise to a high value in the form of a half sinewave ring, as indicated in Fig. 3, as L_Y, C_1 comprise a resonant

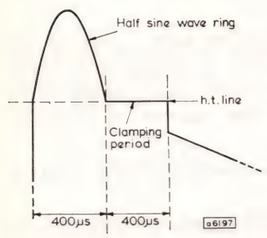


Fig. 3—Voltage at collector of TR_3 during flyback

circuit. As soon as the voltage is reversed and falls to V_{ht} again, D_2 will conduct, and a clamping period will occur until the coil current has been fully reversed.

In effect, it is the energy stored in the scanning coils that must be used for current reversal, but because of the resistive losses in the scanning coils, and external circuitry, it is not quite sufficient. A clamping period where the effective battery voltage across C_4 is connected across the deflection coils is necessary to compensate for these losses and complete the reversal of the scanning current.

Resistors R_2, R_3, and R_5 in Fig. 2 are chosen for correct operation during flyback, and they also provide the necessary d.c. bias irrespective of the a.c. waveform present at the emitter of TR_4. Feedback for linearity correction can be obtained from R_6; the feedback is applied to the junction of C_2 and C_3.

scanning coils, causing an unwanted component of d.c. shift. This effect has been avoided in the complete circuit of Fig. 4 by using a separate bootstrap network, C_4, D_3, R_1, and R_2, to provide the necessary base drive to TR_4. The principle of operation remains the same.

To obtain a variable d.c. shift, the coil-coupling capacitor C_4 in Fig. 2 has been changed from its original position to that shown by C_7 in Fig. 4.

Adjustment of R_{10} will now enable current in the deflection coil to flow in either direction, providing a smooth d.c. shift of the picture up or down.

The flyback switch is a blocking oscillator because of its good interlace characteristics and independent control adjustments. A further advantage is that, by the addition of a small overwind on the collector winding, the means for backing-off are provided to counteract the 'sit-up' voltages that are in the direct coupling path to the base of the output transistor; that is, the base-emitter voltage of TR_2, the forward voltage across D_2, and the collector-emitter voltage of TR_1.

If the e.h.t. supply is unstabilised, to maintain the correct picture aspect ratio with mains and beam-current variations the supply to the charge capacitors (C_2, C_3) is taken from a d.c. potential obtained by rectifying the pulse voltage appearing across the line transformer.

The driver TR_2 is an emitter follower which is bottomed

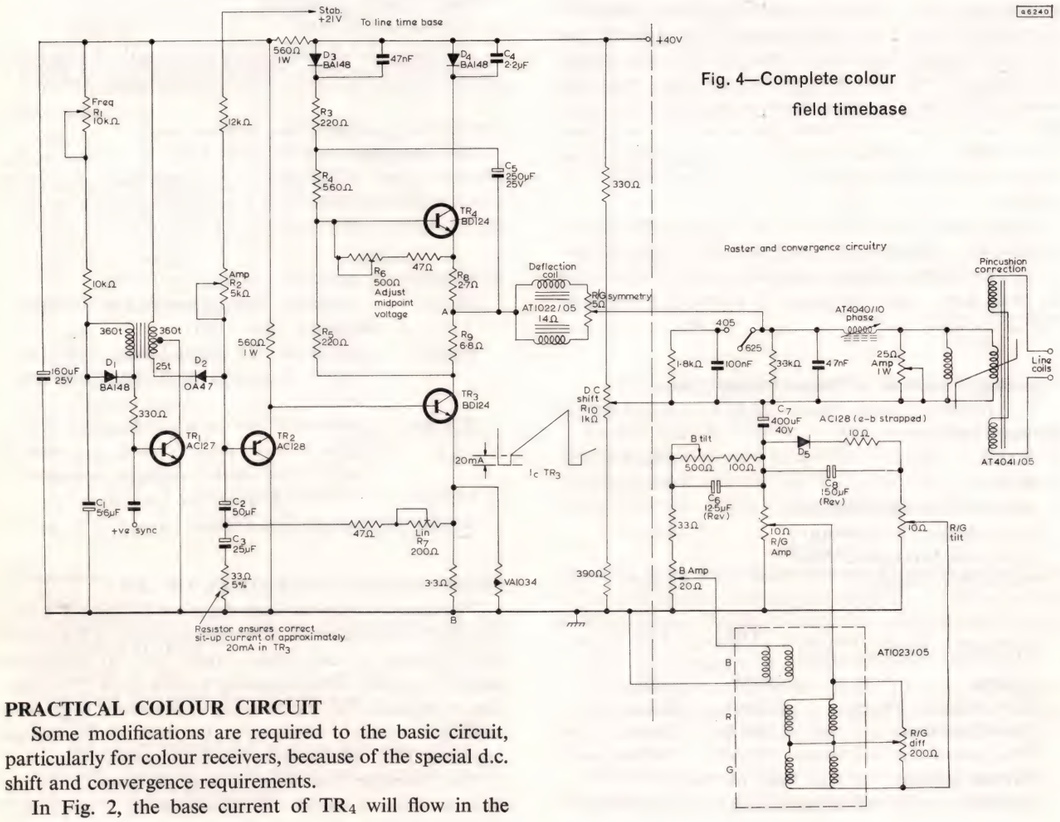


Fig. 4—Complete colour field timebase

PRACTICAL COLOUR CIRCUIT

Some modifications are required to the basic circuit, particularly for colour receivers, because of the special d.c. shift and convergence requirements.

In Fig. 2, the base current of TR_4 will flow in the

during flyback periods. This configuration gives a low dissipation in the driver transistor, and firmly clamps the base of the output transistor to chassis potential at each cycle. Furthermore, any change in the base-emitter voltage of the driver transistor with temperature opposes that of the output circuit, thus providing stability of the working point with temperature.

The charge and timing capacitors must be of a good quality type whose capacitance is stable with life and temperature. It is also important that the charge capacitors have a low series resistance.

In the experimental circuit two types of capacitor have been used which on the life test information at present available give a satisfactory performance.

C_1 Mullard 121 16568
C_2 Mullard C426AR/G50
C_3 Mullard C426AR/F25

C_2 and C_3 should be within $\pm 20\%$ of nominal value.

Field Dynamic Convergence

Satisfactory field dynamic convergence can be obtained by applying the sawtooth current flowing in the field deflector coils through suitable shaping circuits to the field convergence coils.

The circuit shown in Fig. 4 is connected in series with the field deflection coils, and a sawtooth waveform is supplied to the Red/Green convergence coils by the R/G amplitude control. The Red/Green convergence waveform is then modified by sampling the combined sawtooth and parabola voltage developed across the R/G tilt control. A clipping diode D_5 improves the parabolic waveform developed across C_8 and also serves to clamp the centre R/G convergence. A differentiated waveform is applied to the Blue convergence coils by the B amplitude control, and a sawtooth component is added to this by the B tilt control.

Capacitors C_6 and C_8 should be reversible electrolytic types with a tolerance on capacitance of not greater than $\pm 20\%$ and an a.c. voltage rating of not less than 6V peak to peak. Low series resistance is essential, particularly for C_8 ($< 0{\cdot}5\Omega$).

Operating Conditions of Output Circuit (Colour)

The following measurements apply to nominal BD124 output transistors:

E.H.T.	25kV
H.T.	40V
Measured pk–pk deflection coil current (3% overscan)	882mA
Total field timebase current drawn from supply	315mA

	TR_3	TR_4
Maximum collector-emitter voltage	64V*	30V†
Peak collector current	550mA	480mA
'Sit-up' current	20mA‡	20mA
Dissipation	2·9W	3·0W

*during flyback †end of scan
‡at start of scan (no current during flyback period)

Setting-up Procedure

During receiver manufacture, the height control should be set for minimum scan (that is, maximum resistance value) and the rest of the controls should be set to the mid-point of their range. The sequence of setting-up operations is:

(i) Adjust the frequency control until the circuit is synchronised;
(ii) Adjust linearity control for good linearity of scan;
(iii) Adjust height and d.c. shift controls for correct 3% overscan and picture centring;
(iv) Adjust the mid-point voltage control R_6 until the voltage between the transistor end of the scanning coil (point A) and the negative line (point B) is 22V;
(v) Readjust the height and linearity, if necessary;
(vi) Carry out field dynamic convergence.

Components

Deflection coils

The timebase design is based on the Mullard deflection unit type AT1022/05, the field coils being connected in series parallel. Measurements taken on the coil are:

Inductance at 1kHz	24mH
Resistance at 20°C	14Ω
Peak-to-peak current for edge-to-edge scan at 25kV	855mA
Peak-to-peak current for 3% overscan at 25kV	882mA

No thermistor is required in series with the coils (in contrast to the valve field timebase circuit given in Ref. 1.).

Convergence and pincushion corrector units

The convergence unit used with the design is the Mullard type AT1023/05. For pincushion distortion correction, the Mullard unit type AT4041/05 is used with the Mullard variable inductor AT4040/10.

Specification for blocking oscillator transformer

Bobbin	Insulating Components and Materials Limited, type 218A.
Core	$\frac{3}{16}$in stack (14 pairs) Linton and Hurst, Unisil 56, type 218; 0·013in fully interleaved.
Winding	360 turns 2 × 44 s.w.g. self-flux F (BSB188), bifilar wound, plus 25 turns, one winding only; layer-wound without interleaving.
Suitable transformer	Hinchley Engineering Co. Ltd. Sample No. 7994C.

MONOCHROME OPERATION, 110° 20kV

The circuit which has been described for colour is also suitable for monochrome operation with only a few minor modifications to the circuit values and an additional linearity control. This is necessary since more 'S' correction is required for the monochrome picture tube. This additional control, which is in the base of the output transistor TR_3, affects the end of scan linearity (Fig. 5).

The bootstrap system of driving the base of TR_4 is retained since it avoids the unwanted d.c. component.

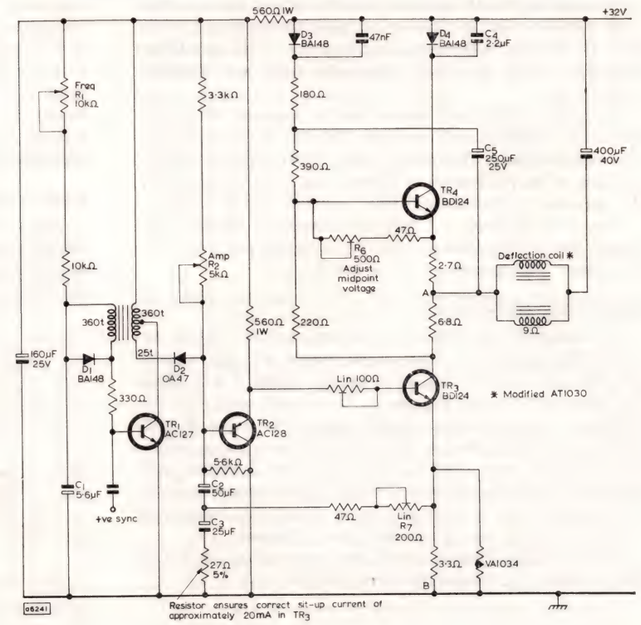


Fig. 5—Complete monochrome field timebase

Setting-up is as for the colour circuit, with the exclusion of (vi) and adjustment of R_6 to 18V instead of 22V.

Operating Conditions of Output Circuit (Monochrome)

The following measurements apply to nominal BD124 output transistors:

e.h.t.	20kV
h.t.	32V
Peak-to-peak deflection coil current (3% overscan) AT1030	1·08A
Total field timebase current drawn from supply	295mA

	TR_3	TR_4
Maximum collector-emitter voltage	65V*	23V†
Peak collector current	610mA	580mA
'Sit up' current start of scan (no current during flyback period)	20mA‡	20mA
Dissipation	3·4W	2·2W

*during flyback
†end of scan
‡at start of scan (no current during flyback period)

Components

Deflection coils

Experimental type. The coils are connected in parallel.

Inductance at 1kHz	20·5mH
Resistance at 20°C	9Ω
Peak-to-peak current for 3% overscan at 20kV	1·08A

No thermistor is required in series with the coils.

Blocking oscillator transformer and capacitors C_1, C_2, and C_3 as for colour circuit.

BLANKING CIRCUIT

Blanking is applied by means of a series transistor in the cathode circuit of the valve luminance amplifier for colour receivers (Fig. 6). For monochrome sets with transistor video output stages the circuit is connected in series with the emitter of the video output transistor.

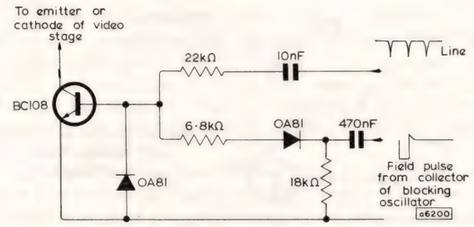


Fig. 6—Combined field and line blanking circuit

During flyback a low-level pulse is obtained from the blocking oscillator and applied to the base of the series transistor such that the valve or transistor video stage is cut off for the whole of the blanking period.

APPENDIX

Operation of the Single-ended Push-pull Circuit During Flyback

In field circuits employing transformer or choke output configurations, complete reversal of the deflection coil current is easily obtained because of the extra stored energy available in the choke or transformer.

In transformerless/chokeless circuits, however, flyback is more difficult to achieve since no additional inductor is present to store energy. It is thus necessary to utilise the scanning coil inductance itself as the main current reversal source.

It becomes imperative that the stored energy in this inductance be used as efficiently as possible and not dissipated in

components or devices that contribute nothing to flyback. This is the reason for the voltage step during flyback imposed on the base of the lower output transistor since it cuts off this device extremely rapidly ($< 10\mu s$). Dissipation losses are therefore virtually zero.

Adequate flyback performance can be obtained with transformerless output circuits provided that the circuit configuration and component values are correct. This requires an understanding of the mechanism of flyback, and it is the purpose of this appendix to discuss the flyback operation in some detail.

Fig. 4 will be used as a basis for component numbers discussed, and numerical values, where quoted, will relate to 25kV 90° colour tube operation from a 40V h.t. rail.

PART ONE OF FLYBACK

It is assumed that flyback is just commencing; that is, the switch TR_1 is closed and the output transistor is just cutting off. The sequence will then be as follows. Point A will firstly rise very fast positive because of the stored energy in the deflection coil inductance. At the instant that point A goes substantially above the h.t. rail, diodes D_3 and D_4 go into a nonconductive state, and C_4 tunes with the deflection coil inductance to form a resonant circuit at field flyback frequency. Consequently the voltage rises in a sinusoidal manner as shown in Fig. 7a, and allows fast current reversal.

The equivalent output circuit then becomes as shown in Fig. 8, where C_5, being large, is in effect a battery.

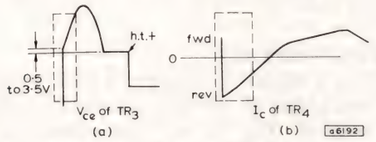


Fig. 7—V_{ce} of TR_3 and I_c of TR_4 during flyback. Dashed lines show part considered in 'Part 1 of flyback'

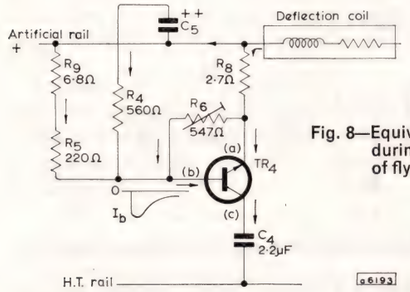


Fig. 8—Equivalent circuit during Part 1 of flyback

Transistor TR_4 is now operating in a reverse conduction mode and the necessary base current is predominantly supplied by R_4 in Figs. 4 and 8 (although R_5 and R_9 do have some influence due to the voltage drop across R_8). Ideally, this current should be sufficient to ensure that the transistor TR_4 is bottomed under the maximum reverse current condition occuring at the start of the flyback stroke. To ensure that this is so would require unnecessarily stringent base network values or a guaranteed high reverse mode current gain in TR_4. Assume, therefore, that the base current is insufficient to support the 'new collector' current (terminal (a) Fig. 8), the collector-emitter voltage will rapidly increase as a result, thus more current will flow via R_4, R_9, and R_5, and additionally via R_6 until the collector current *can* be supported. The circuit thus stabilises itself against wide spreads of reverse h_{FE}. In the colour circuit, by way of example, a reverse collector-emitter voltage of 3·5V during this instant of flyback will cater for transistors with reverse current gains down to 5. The effect of this voltage on TR_4 dissipation is negligible, only amounting to additional dissipation in the mW region. Alternatively, a diode may of course be used in shunt with TR_4, to allow the reverse current to flow, but since the device used for TR_4 has been made suitable for this mode of operation, the cost of a high-current shunt diode is saved.

PART TWO OF FLYBACK

Part two starts as the sinusoidal coil voltage reverses and its current passes through zero. Transistor TR_4 works in a conventional manner from this instant and for the remainder of the flyback and scanning cycle.

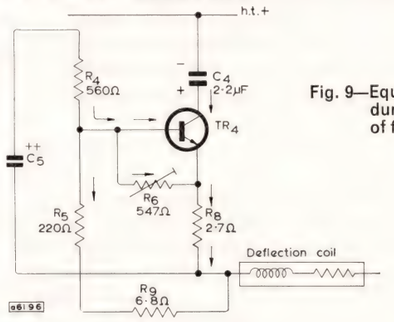


Fig. 9—Equivalent circuit during Part 2 of flyback

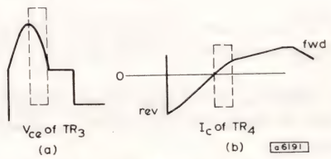


Fig. 10—V_{ce} of TR_3 and I_c of TR_4 during flyback. Dashed lines show part considered in 'Part 2 of flyback'

The equivalent circuit is shown in Fig. 9. For low currents in TR_4 the base current is mainly determined by R_4 and 'battery' C_5, TR_4 being bottomed. As the collector current increases, the battery voltage across C_5 is fixed, but a voltage is progressively developed across R_8 in opposition, thus base current decreases as the collector current increases.

PART THREE OF FLYBACK

During part three the sinusoidal flyback voltage continues to drop until the collector of TR_4 becomes clamped to the h.t. rail by conduction of diode D_4 (Fig. 11) and a clamping period then occurs (see Fig. 12a).

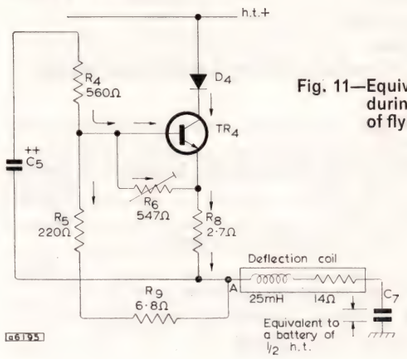


Fig. 11—Equivalent circuit during Part 3 of flyback

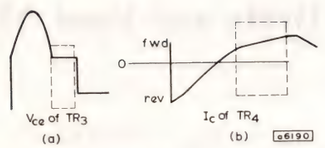


Fig. 12—V_{ce} of TR_3 and I_c of TR_4 during flyback. Dashed lines show part considered in 'Part 3 of flyback'

This clamping period is necessary, since, as can be seen from Fig. 12b, the deflection coil current has not fully reversed (because of the losses within the deflection coil circuit) at the end of the resonant voltage swing considered in parts one and two of flyback.

From Fig. 11 it can be seen that the prime cause of continuing reversal of the deflection coil current will be the h.t. rail voltage minus the effective battery voltage across C_7, this resultant voltage being clamped across the coils until the current has fully reversed. (Voltage drops across D_4, TR_4, and R_8 are small and have been neglected.)

By way of example, the colour circuit results in a clamping voltage of approximately 18V across the 14Ω deflection coils during this period. Thus the aiming current will be 18/14A $\simeq$ 1·3A over a period dependent on the LR time constant of the deflection circuit.

It has already been mentioned in part two of the flyback that as the collector current in TR_4 increases the base current reduces because the increasing voltage across R_8 causes the available current from C_5 and R_4 to divide between the base path and R_5. The base path also has a shunt resistance R_6 between base and emitter, so the effective base current can be reduced at will, by reducing the value of R_6.

It follows, therefore, that as the collector current is increasing and base current is reducing there will be a point at which the collector current can no longer be supported by the available base current. This point in time can be controlled by adjustment of R_6, hence the clamping period and thus flyback time can be altered within certain limits according to the application and systems requirements.

PART FOUR OF FLYBACK

Part four covers the end of flyback and the start of the scanning stroke.

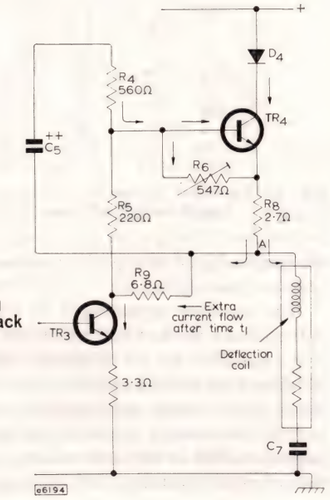


Fig. 13—Equivalent circuit during Part 4 of flyback

Part three has established that as the collector current of TR_4 increases its base current falls, and a time arises when the base current can no longer support the collector current. No more base current can be supplied since C_5 (Fig. 13) is a battery source and all resistors are fixed.

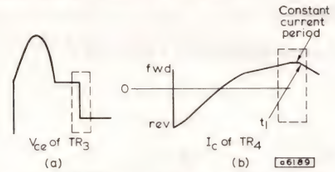


Fig. 14—V_{ce} of TR_3 and I_c of TR_4 during flyback. Dashed lines show part considered in 'Part 4 of flyback'

As a result TR_4 starts to come out of bottoming and rapidly becomes a constant current generator (that is, I_b remains constant irrespective of V_{ce} since the base drive network is an effective battery network between emitter and base). The situation has arisen, therefore, where during the clamping period a voltage of $V_{ht}-(V_{ce(TR4)}+V_{D4}+V_{R8}+V_{C7})$ is clamped across the coils ($\simeq$18V for the colour circuit). When the base current no longer supports the collector current at the predetermined level of say 0·45A, the effective voltage generator across the coils suddenly becomes a constant current generator of 0·45A. The voltage across the coils will, therefore, immediately drop to that value determined by the resistance of the coils and the relevant current; that is, $14\Omega \times 0{\cdot}45A = 6{\cdot}3V$, the inductive component voltage drop across the coils immediately becoming zero.

This explains the voltage step in the flyback waveform shown in Fig. 14a, and also why no ringing occurs, since the magnetic flux remains unaltered during this transitional step period.

In the example quoted this step voltage will be approximately $18-6{\cdot}3V = 11{\cdot}7V$.

Since the base network of TR_4 is being supplied by the battery C_5, controlling the constant generator TR_4, the deflection coil current will be maintained constant (at say 0·45A) until such time as either TR_3 starts to conduct and alters the bias levels on TR_4 or, in the limit, if TR_3 was non-conductive and the time constant of the effective C_5 battery network is approached.

In general the conduction of TR_3 (which is controlled by the pulse duration of the blocking oscillator switch TR_1) is made to begin equal to or even slightly longer than the period needed to fully reverse the scanning coil current.

From the foregoing it might be thought that the flyback time would be very dependent on the h_{FE} of TR_4, and that critical adjustment of R_6 is required.

In terms of flyback time this is not so, however, since even under maladjustment conditions if the clamping period tended to become too long, the conduction of TR_3 (which is carefully controlled by TR_1) would force the flyback to end. Correct timing would thus be ensured with an error dependent only on the spread in TR_1 conduction time.

Practical results indicate that flyback times down to 650μs are possible, with suitable h.t. rails and the techniques described. In addition, these flyback times are quite repeatable even in large-scale production.

REFERENCE AND ACKNOWLEDGEMENTS

1. BOULTON, P. G. 'Field Timebase'. **Mullard Technical Communications,** Vol. 9, No. 83, Sept. 1966, pp. 67 to 69.

Acknowledgements are due to D. King who carried out additional work on the convergence circuitry.

Electronic Speed Control for Electric Drills and Food Mixers

R. P. GANT

Mullard Central Application Laboratory

Two simple motor speed control circuits are described and their characteristics compared. The shortcomings of these circuits are the limited control range and roughness of operation at low speeds. An improved circuit is described that has a speed control range of some 5 : 1 with smooth operation and good torque/speed characteristics. Design information is given for matching a control system to a motor for optimum performance.

INTRODUCTION

Both electric hand drills and food mixers are appliances that need to have several operating speeds to perform their different functions.

In the circuit to be described continuous speed control over a wide speed range is effected by using a thyristor whose conduction angle is varied to obtain different motor speeds. Motor speed is in turn maintained by feedback from the motor residual back e.m.f.

A voltage ramp of low slope whose d.c. level may be varied is a feature of the circuit that allows a maximum phase angle change with minimum speed drop at all motor speeds. The use of this circuit also results in smooth motor operation which is an advantage over other simple electronic speed control circuits that are also described.

BACK E.M.F. FEEDBACK CIRCUITS

To maintain motor speed under changing conditions of motor load or mains supply voltage the motor back e.m.f. is used to change the thyristor triggering angle.

A simple motor speed control circuit that employs this technique is shown in Fig. 1. The resistor chain R_1, R_2, R_3 and diode D_1 provide a positive going reference potential to the thyristor gate via diode D_2. Diode D_1 is used to reduce the dissipation in the resistor chain by some 50%, and diode D_2 isolates the trigger circuit with the thyristor in the on-state. When the thyristor is not conducting the motor produces a back e.m.f. across the armature proportional to residual flux and motor speed. This appears as a positive potential at the thyristor cathode.

The thyristor triggers when the gate potential is greater than the cathode potential by some fixed amount. Depending on the waveform shape and amplitude at the gate, the circuit may function in several modes.

If, for example, during positive half cycles a constant d.c. potential was applied at the gate (Fig. 2), the thyristor would continue to trigger at the beginning of each cycle until the back e.m.f. was large enough to prevent triggering. Thyristor triggering would then continue intermittently at the beginning of the positive cycles to maintain some average motor speed.

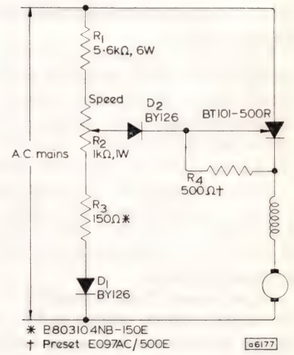


Fig. 1—Simple speed control circuit. Values of R_2 and R_3 depend on motor back e.m.f. and minimum speed required

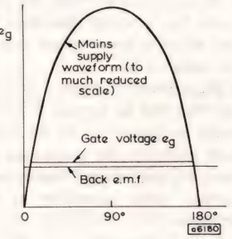


Fig. 2—Potentials at thyristor gate during positive half cycles

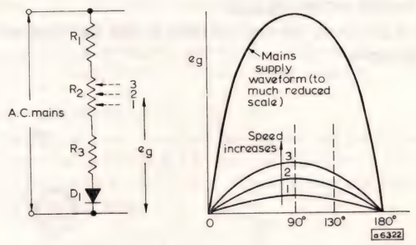


Fig. 3—Waveform appearing at thyristor gate for various speed control settings of Fig. 1 circuit

The waveform appearing at the thyristor gate in Fig. 1 will approximate to a half sine wave (Fig. 3). As a result it is impossible for the triggering angle to be later than 90° (the most positive value of the trigger potential). At lower motor speeds the triggering angle might typically be 130° for smooth operation, so that if the maximum angle is limited to 90°, intermittent triggering and roughness of motor operation will inevitably result.

If, however, the waveform at the gate has a positive slope value to an angle of at least 130° a stable triggering point will be achieved at low speeds. Such a waveform requires some phase shift in the trigger network.

STABLE TRIGGERING AT SMALL CONDUCTION ANGLES

The trigger network shown in Fig. 4 has been modified by the addition of a capacitor C_1 and diode D_1. The diode clamps the capacitor potential at zero during the negative-going half cycles of the mains input. The waveform developed across the capacitor has a positive slope to some 140° so permitting stable triggering to this point at low motor speeds.

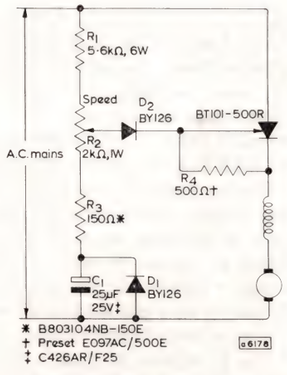


Fig. 4—Modified speed control circuit. Values of R_2 and R_3 depend on motor back e.m.f. and min speed required. C_1 voltage rating depends on motor back e.m.f.

As the slider of R_2 is moved towards R_1 the peak of the waveform at the gate will move towards 90°, as shown in Fig. 5, but as the speed increases the no-load triggering angle will also advance by a similar amount, so maintaining stability. However, although the circuit gives smoother

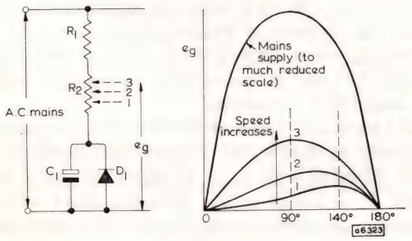


Fig. 5—Waveform appearing at thyristor gate for various speed control settings of Fig. 4 circuit

or more stable performance than that of Fig. 1, it will give a marginally greater speed drop for a given motor loading at low speed settings. At the maximum speed settings the circuit of Fig. 4 approximates to that of Fig. 1.

IMPROVED MOTOR PERFORMANCE WITH STABLE TRIGGERING

Both circuits so far discussed have voltage waveforms at the thyristor gate that are of near-linear slope from the zero point of positive half cycles (see Figs. 3 and 5). Thus, to obtain a thyristor conduction angle of 160° (triggering angle of 20°) the back e.m.f. and motor speed will have to fall to a very low value.

The circuit of Fig. 6, however, produces a voltage waveform at the gate, shown in Fig. 7, that in addition to giving a stable triggering point at low speeds, will allow a 160° conduction angle with a minimum speed drop. The gate waveform has a positive slope value from 0° to around 140° in each positive half cycle.

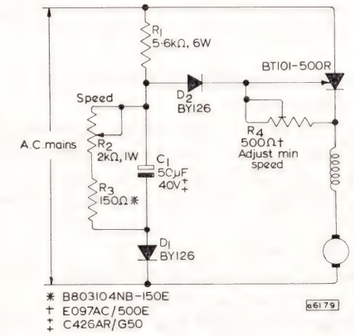


Fig. 6—Improved speed control circuit. Values of R_2 and R_3 depend on motor back e.m.f. and min speed required. C_1 voltage rating depends on motor back e.m.f.

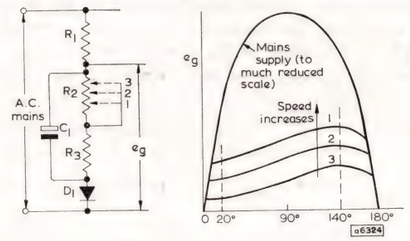


Fig. 7—Waveform appearing at thyristor gate for various speed control settings of Fig. 6 circuit

A low value of positive slope for the triggering waveform is produced by starting each cycle at a positive potential that may be varied by the speed control R_2 without changing the slope value. It may be seen that C_1 is charged during positive half cycles via R_1 and diode D_1. During negative half cycles the only discharge path for C_1 is via R_2 and R_3. Diode D_1 also prevents C_1 from being discharged, as the thyristor switches off, by the inductively generated pulse from the motor. As the value of R_2 is increased, C_1 is discharged less during negative half cycles, but its charge waveform remains substantially unchanged. Hence the result of varying R_2 is to shift the d.c. level of the ramp waveform produced across C_1.

Diode D_2 isolates the triggering circuit with the thyristor in the on-state. Resistor R_4 adjusts minimum speed, and by bleeding effectively a constant current in conjunction with the gate current from the triggering circuit enables R_2 to give consistent speed settings.

CIRCUIT DESIGN

It is desirable that a food mixer or a hand drill speed control has stable thyristor triggering angles at all speeds, and gives the best possible speed regulation with variations

of motor load. The circuit of Fig. 6 gives a motor performance that satisfies both of these requirements.

There are two factors that are important in the circuit operation if the above requirements are to be satisfied:

(i) the value of positive slope of the waveform appearing at the thyristor gate;
(ii) the phase angle at which the positive peak gate voltage is reached during a positive half cycle of mains input.

As previously described, the charging of C_1 by R_1 (Fig. 6) determines the rate of rise of voltage at the thyristor gate during the positive half cycle. Resistor R_1 must, however, also have a value such that several times the maximum thyristor gate current passes through the R–C network to D_1. This current will then give consistent speed settings with the spread of thyristor gate currents when the minimum speed is set by R_4.

The positive slope value of the thyristor gate voltage will have to be fixed according to the motor used. A motor that gives a smooth back e.m.f. will allow a low slope value to be used, giving good torque/speed characteristics. Some motors have coarser back e.m.f. waveforms with voltage undulations and spikes, and a steeper slope of thyristor gate voltage must be used to obtain stable motor operation. The value of C_1 is chosen to provide the required positive slope of the thyristor gate voltage.

Some calculations have been made on the circuit of Fig. 6 simplified to the form of Fig. 8, where it is assumed that current flowing to the thyristor gate is small compared with the current flowing through R_1. An expression has

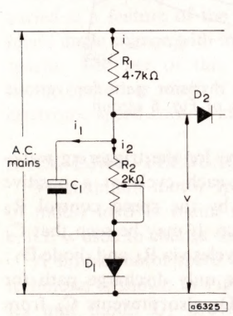


Fig. 8—Simplified thyristor triggering circuit

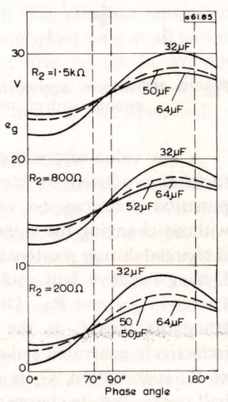


Fig. 9—Calculated gate waveforms for various values of R_2 and C_1

been derived for the voltage that would appear at the anode of D_2 in terms of resistors R_1, R_2, R_3, and C_1, and is given in the Appendix. Component values have been substituted into the expression to give the thyristor gate waveforms shown in Fig. 9.

To adjust the circuit to suit a given motor, the remanent back e.m.f. of the motor must be measured. This may be carried out as shown in Fig. 10. The voltage appearing across the motor is measured during the period when the series diode is not conducting (period A). The voltage so

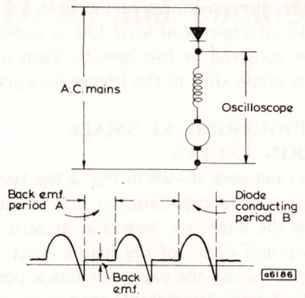


Fig. 10—Measurement of series motor back e.m.f., showing typical waveform

obtained will be the back e.m.f. at top motor speed on half-wave operation, and corresponds to the back e.m.f. that would be obtained from the unloaded motor at its highest speed when thyristor controlled. In practice, since the mains input is a sine wave, little speed increase occurs (no load) with triggering angles smaller than about 70°.

The value of R_2 in Fig. 6 determines the motor no-load speed setting. The waveforms of Fig. 9 may be used as a guide to obtaining the value of this resistor. It must be chosen so that at 70° and at its highest value, the gate voltage is higher than the measured back e.m.f. by about 2V (the forward gate-to-cathode voltage of the thyristor).

The thyristor triggers when a trigger waveform, shown in Fig. 9, exceeds the back e.m.f. by the gate-to-trigger voltage. Hence if the back e.m.f. has well-defined variations during one half cycle, as opposed to high-frequency commutator noise, variations of the triggering angle will occur from cycle to cycle.

Random variations of the triggering angle by 20° are usually tolerable. If, for instance, there were variations of back e.m.f. of 1·0V at a triggering angle of 70°, with C_1 at 32μF the variation of triggering angle would be about 12°. With capacitor values of 50μF and 64μF the variations would be 19° and 25° respectively. A capacitor value of 50μF would then be suitable.

For a particular type of motor the value of R_3 (minimum speed) may be determined by inserting a high-limit gate current thyristor with R_4 at its maximum value. Subsequently R_4 is preset at the minimum speed setting to compensate for spread of the thyristor gate characteristic.

PERFORMANCE

The torque/speed characteristics of the three circuits described, when employed in a hand drill, are compared in Fig. 11. It may be seen that the circuit of Fig. 4 has a poorer performance than the two other circuits. That of Fig. 6 may be seen to give a similar performance to the circuit of Fig. 1 at the lower speed, but it shows an improvement at higher speed at the higher torques. It must also be taken into account that the circuits of Figs. 4 and 6 provide low-speed operation free from the intermittent triggering and the resulting noise that are characteristic of Fig. 1.

Fig. 12 shows the torque/speed curves of the circuits of Figs. 1 and 6 used to control a food mixer.

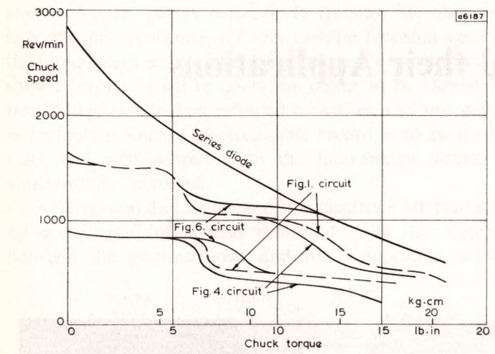


Fig. 11—Torque/speed curves of 180V hand drill motor controlled by circuits of Figs. 1, 4, or 6 working at 240V. Residual back e.m.f. is 5V at chuck speed of 2800 rev/min. Gearing ratio is 7 : 1

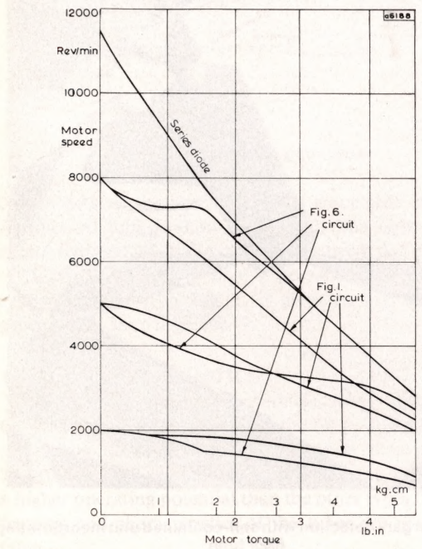


Fig. 12—Torque/speed curves of 180V food mixer motor controlled by circuits of Figs. 1 or 6 working at 240V. Residual back e.m.f. is 20V at motor speed of 10 000 rev/min

APPENDIX
Calculations for the Circuit of Figure 8

The charging current i_1 for capacitor C_1 (Fig. 8) is given by:

$$i_1 = dq/dt = C(dv/dt)$$

and

$$i_2 = v/R_2.$$

If we represent a mains half sine wave by f(E), where E is peak mains voltage, then

$$i = [f(E)-v]/R_1 = i_1+i_2$$

therefore

$$[f(E)-v]/R_1 = C(dv/dt)+v/R_2$$

where i, i_1, i_2 are instantaneous currents. This expression can be simplified to:

$$C\frac{dv}{dt}+v\left(\frac{1}{R_1}+\frac{1}{R_2}\right)=\frac{f(E)}{R_1}.$$

Fourier analysis of a half sine wave gives:

$$f(E)=E\left[\frac{1}{\pi}+\frac{1}{2}\sin\theta-\frac{2}{\pi}\sum_{n=2,\,4,\,6\ldots}^{n=\infty}\frac{\cos n\theta}{n^2-1}\right].$$

If we neglect the terms of the fourier series with $n > 2$, then

$$C\frac{dv}{dt}+v\left(\frac{1}{R_1}+\frac{1}{R_2}\right)=\frac{E}{R_1}\left(\frac{1}{\pi}+\frac{1}{2}\sin\omega t-\frac{2}{3\pi}\cos 2\omega t\right)$$

and

$$C\frac{dv}{dt}+v\left(\frac{1}{R_1}+\frac{1}{R_2}\right)-\frac{E}{R_1\pi}=\frac{E}{R_1}\left(\frac{1}{2}\sin\omega t-\frac{2}{3\pi}\cos 2\omega t\right) \quad \ldots(1)$$

which can be simplified to:

$$A(dv/dt)+Bv-D = X\sin\omega t-Y\cos 2\omega t \quad \ldots(2)$$

where A, B, D, X, Y are constants.

If we make

$$v = a\sin\omega t+b\cos\omega t+c\sin 2\omega t+d\cos 2\omega t+D/B \quad \ldots(3)$$

where a, b, c, d are constants, then

$$dv/dt = a\omega\cos\omega t-b\omega\sin\omega t+2c\omega\cos 2\omega t-2d\omega\sin 2\omega t \quad \ldots(4)$$

Substitution of (3) and (4) in (2), and equating of terms in $\cos\omega t$, $\cos 2\omega t$, $\sin\omega t$, $\sin 2\omega t$, gives:

$$v=\frac{BX}{A^2\omega^2+B^2}.\sin\omega t-\frac{A\omega X}{A^2\omega^2+B^2}.\cos\omega t-\frac{2A\omega Y\sin 2\omega t}{4A^2\omega^2+B^2}-$$
$$-\frac{BY}{4A^2\omega^2+B^2}.\cos 2\omega t+\frac{D}{B}.$$

Substitution for the constants in (2) gives:

$$v=R_2E\left[\frac{(R_1+R_2)\sin\omega t-\omega CR_1R_2\cos\omega t}{2\omega^2c^2R_1^2R_2^2+(R_1+R_2)^2}+\frac{1}{\pi(R_1+R_2)}-\right.$$
$$\left.-\frac{4\omega CR_1R_2\sin 2\omega t+4(R_1+R_2)\cos 2\omega t}{3\pi[4\omega^2c^2R_1^2R_2^2+(R_1+R_2)^2]}\right].$$

This may be simplified, since $(R_1+R_2)^2$ is much less than $2\omega^2c^2R_1^2R_2^2$.

Hence

$$v=\frac{R_2E}{\pi(R_1+R_2)}+\frac{R_2E}{2\omega^2c^2R_1^2R_2^2}\left[(R_1+R_2)\sin\omega t-\right.$$
$$-\omega CR_1R_2\cos\omega t-\frac{2}{3\pi}\omega CR_1R_2\sin 2\omega t-$$
$$\left.-\frac{2}{3\pi}(R_1+R_2)\cos 2\omega t\right].$$

Diode Image Converter Tubes and their Applications

K. A. COOK
Mullard Industrial Electronics Division

Diode image converter tubes convert an input pattern of near-infrared radiation into a visible output pattern allowing visual observation or photographic recording of phenomena without the use of light. Operation of the tubes is described, high-voltage supply circuits are given for portable self-contained units, and practical set-ups are outlined. As an example, infrared observation of ant behaviour is briefly described.

INTRODUCTION

Diode image converter tubes, such as the Mullard 6914, 6929, and 6929-1, operate with a near-infrared input and provide a visible image at the output. They are therefore suitable for three classes of application:

(i) Observation of phenomena where the presence of light would modify the phenomena. Examples are examination of the eye without excitation of its normal reflex responses (such as contraction of the pupil), and observation of animal life.

(ii) Observation of phenomena that would not be observable, or readily observable, without the use of infrared radiation. Examples are detection of refractory faults in furnace walls (thermal insulation breakdown); monitoring of infrared lasers or gallium arsenide electroluminescent diodes; detection of hot-spots (such as overheated resistors in electronic apparatus, overheated axle-boxes on railway trains, and leaky insulators on power lines); and detection of alterations made to cheques (Fig. 1), examination certificates (Ref. 1) or other documents. Hot-spots at temperatures below 350°C are more readily observed by means of semiconductor detector devices.

(iii) Observation of phenomena where the presence of light, although technically unobjectionable, is undesirable for other reasons. Examples include military observation and crime detection.

An application from the first group will be discussed as an illustrative example of the potentialities of diode image converters (page 258).

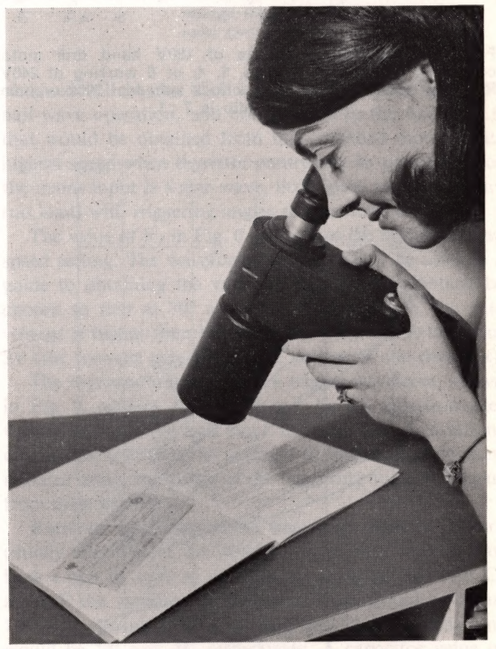


Fig. 1—Forgery detection with self-contained unit incorporating 6929 tube

STRUCTURE AND OPERATION

The diode image converter tube consists of a photocathode and a luminescent screen. A near-infrared 'image' is focused on to the photocathode by a conventional optical system. Each point on the photocathode emits electrons in proportion to the infrared radiation incident at that point. The electrons are automatically focused by a high-voltage electrostatic lens on to the luminescent screen, which provides a visible image of the original infrared 'picture'. An optical eyepiece magnifies this image. The two optical systems do not form part of the tube; they must be provided by the user.

Fig. 2 shows the elements of one practical system. The observed object is irradiated by an infrared source,

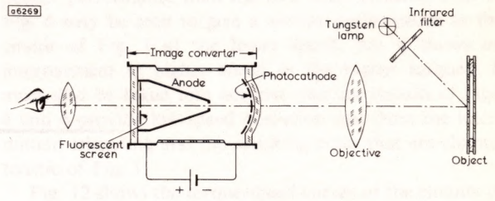


Fig. 2—Infrared viewing system

and its 'image' passes successively through the objective lens, the photocathode, the electrostatic focusing system, the luminescent screen, and the eyepiece. The arrangement shown can be varied to allow the object to be viewed by transmitted rather than reflected radiation; this procedure is preferable when a photographic record is to be made, since the light output from the luminescent screen is substantially increased.

Acceleration and focusing of the electrons are provided by a potential of several thousand volts d.c. applied between the photocathode and the luminescent screen

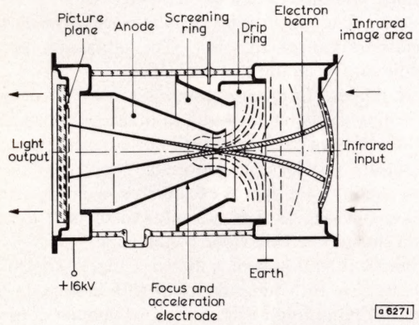


Fig. 3—Diode image converter

(which acts as the anode) with its associated structures. A practical tube is shown in Fig. 3. The only electrical circuit required is a high-voltage low-current d.c. generator.

A practical realisation of a portable infrared viewing system, as shown in Fig. 1, is given in Fig. 4. The h.t. generator is shown in Fig. 7.

TUBE CHARACTERISTICS

Three diode tubes are available from Mullard: the 6914; a physically smaller tube, the 6929; and the 6929-1, which has rather less screen resolution than the 6929. The tubes are all structurally similar, but the 6914 requires a higher operating potential than the other types. The main features and characteristics of the tubes are given in the table.

	6914	6929	6929-1	
Photocathode				
Min useful diam.	25·4	19	19	mm
Area	5·06	2·84	2·84	cm^2
External radius of curvature	60	31	31	mm
Luminescent screen				
Min useful diam.	19·3	14·5	14·5	mm
Typical operating conditions				
Anode voltage	16	12	12	kV
Anode current	20	20	20	nA
Characteristics				
Min conversion coefficient	0·6	0·4	0·4	cd/lm irf
Centre magnification	0·76	0·74	0·74	
Distortion	8·5 to 12·5	5·5 to 10	5·5 to 10	%
Min centre resolution	50	50	35	line pairs/mm

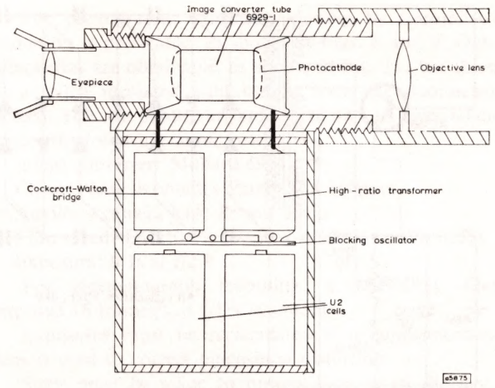


Fig. 4—Portable viewing system

Details of the conditions under which these characteristics are measured, and of the limiting conditions that must be observed, are given in the data sheets for the three types (Ref. 2). It is important that the tubes should not be subjected to excessive voltages or to excessive infrared radiation.

In all three tubes the photocathode is type C, caesium on oxidised silver, with S1 response as shown by curve 1 in Fig. 5. Curve 2 shows the relative spectral radiation

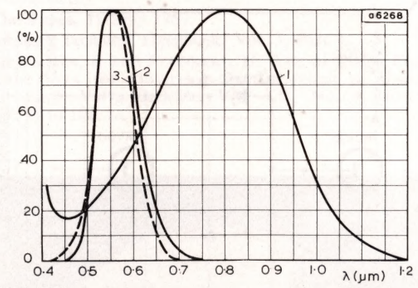


Fig. 5—Response curves
(1) photocathode (2) luminescent screen (3) eye

distribution of the yellow-green KA (P20) luminescent screen. Curve 3 shows the response of the average human eye. Fig. 5 neatly illustrates the shifting of the image from the invisible region to the visible region.

IMAGE DISTORTION

The concave cathode of the tube produces pincushion distortion of the image on the luminescent screen. This is of little consequence in most applications, since the purpose of the application is usually observation and not measurement. However, the distortion can be partly corrected by optically introducing barrel distortion of the image formed on the photocathode. If photographic recording is used, the additional lens must be taken into account when calculating the exposure.

HIGH-VOLTAGE SUPPLY

The current through image converter tubes is very

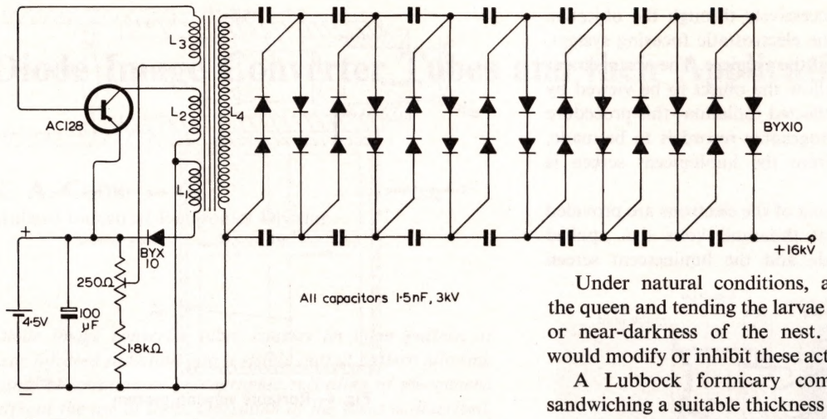


Fig. 6—16kV power supply for 6914

small. The power requirements are:

6914: 320µW 6929: 240µW 6929–1: 240µW

Small, cheap power units are therefore adequate.

One practical circuit, providing 16kV for the 6914, is shown in Fig. 6. The voltage generator is powered by a 4·5V torch battery. This unit is incorporated in the experimental set-up shown in Fig. 9.

An alternative circuit, providing 12kV for the 6929 or 6929–1, is shown in Fig. 7. This is a simple blocking oscillator with a high-ratio transformer that supplies

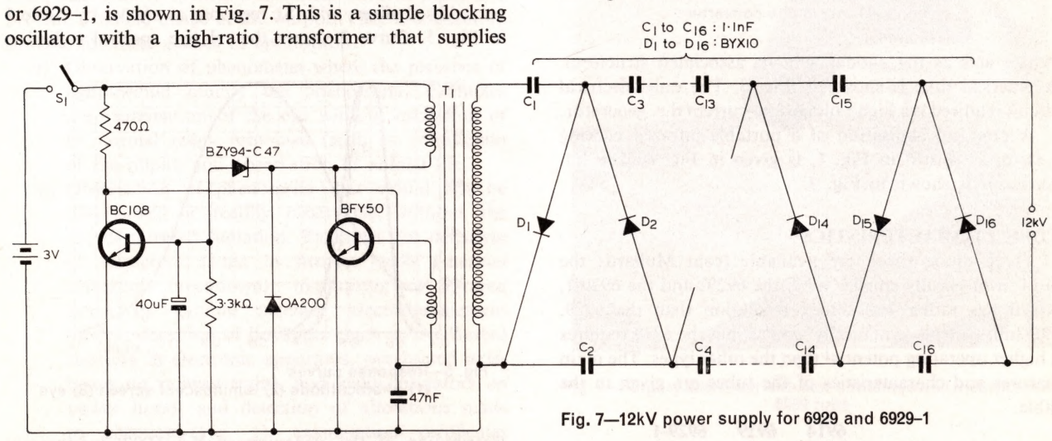


Fig. 7—12kV power supply for 6929 and 6929–1

1·5kV pulses to the eight-stage Cockcroft-Walton bridge. The power for the blocking oscillator is provided by two U2 cells in series. A practical realisation of this circuit is incorporated in the unit shown in Figs. 1 and 4.

Either of the circuits, Figs. 6 and 7, can be adapted to supply the appropriate voltage for any of the tube types. The maximum voltage limits of the tubes, as given in the data sheets, must not be exceeded; but, with that proviso, the voltages applied to the tubes are not critical, and the image sharpness is little affected if the voltage falls by 2 or 3kV.

ILLUSTRATIVE APPLICATION

An interesting application of the image converter tube has been fully described in Ref. 3. The 6914 tube was used for the observation of the yellow meadow ant (*lasius flavus*) in artificial nests known as Lubbock formicaries.

Under natural conditions, activities such as feeding the queen and tending the larvae take place in the darkness or near-darkness of the nest. The admission of light would modify or inhibit these activities.

A Lubbock formicary comprises two glass plates sandwiching a suitable thickness of moist soil in which the ants form nesting cavities but do not escape observation. This set-up provides a reasonable approximation to natural conditions if light is excluded. Viewing by infrared radiation (so long as it is not allowed to heat the nest) will not distort the behaviour of the ants.

A practical arrangement is shown in Fig. 8. The infrared source consists of a tungsten lamp with a suitable filter. In Fig. 9 a hand-torch with a sheet of ebonite is used.

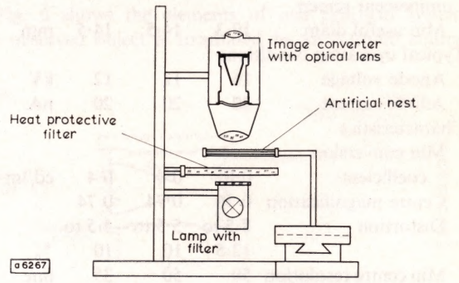


Fig. 8—Observation of artificial nest

Irradiation may be at an angle, producing an image by reflection. The image is relatively faint but sufficiently clear for direct visual observation. Fig. 10 shows a yellow meadow ant viewed in this manner.

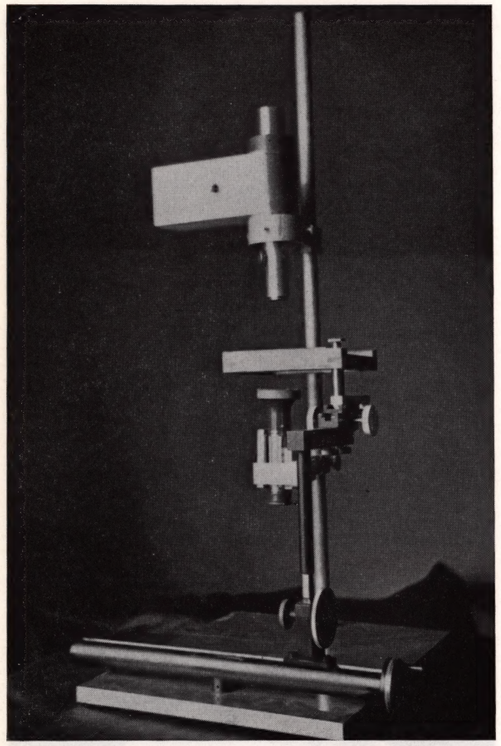


Fig. 9—Practical viewing system for laboratory use

For photographic purposes, viewing by transmitted radiation is preferable, as shown in Figs. 8 and 9. Only silhouettes are obtainable, as shown in Fig. 11; but there is a much increased light output from the fluorescent screen. The two photographs, Figs. 10 and 11, were taken under the following conditions:

Image converter: Mullard 6914
Camera lens: Kontaflex Pantar 1:2·8/45mm
Auxiliary camera lens: Proxar 30cm
Film speed: DIN10/17° (approx ASA 64 or BSI 0252)
Exposure: 0·1s at f/2·8

For cinematograph recording, a DIN10/21° film exposed 16 frames/s at f/1·9 is suitable.

Exposures must be recalculated if a supplementary lens is used to correct pincushion distortion.

Steps must be taken to prevent heating of the nest, especially when prolonged and continuous observation is proposed. An additional heat filter may be used in combination with suitable spacing of nest, source, and filters. A cooling airflow may be used if necessary.

Figs. 12, 13, 14, and 15 show various activities within the nest.

ACKNOWLEDGEMENT

The circuit diagram, Fig. 6, and the photographs, Figs. 9 to 15, are taken from Ref. 3.

REFERENCES

1. **The Times,** 31 May 1967.
2. **Mullard Technical Handbook,** Vol. 3, Part 1.
3. SUHRMANN, R and FLUNKERT, H. 'Use of Image Converter Tube 6914 for Observing the Behaviour of Insects' (in German). **Valvo Berichte,** Vol. XII, No. 4, Nov. 1966, pp. 95 to 104.

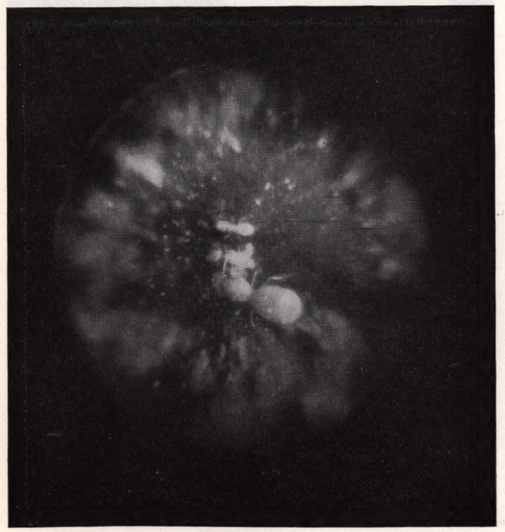


Fig. 10—Yellow meadow ant queen viewed by reflected radiation

Fig. 11—Yellow meadow ant queen viewed by transmitted radiation

Fig. 12—Feeding the queen

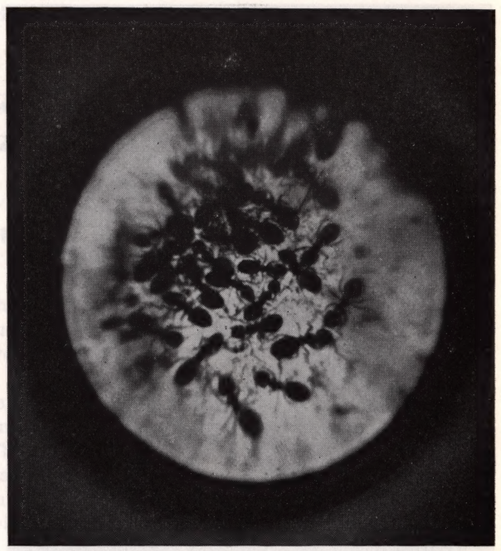


Fig. 13—Workers congregating

Fig. 14—Tending the larvae

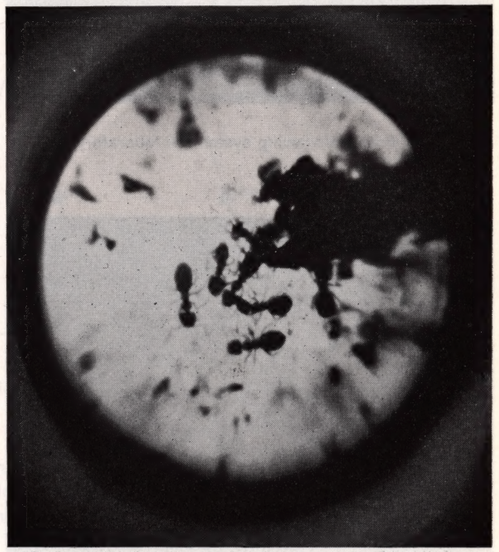


Fig. 15—Workers nest-building